DS21Q55 Quad T1/E1/J1 Transceiver

FEATURES:

Complete T1 (DS1)/ISDN–PRI/J1 transceiver functionality

- Complete E1 (CEPT) PCM-30/ISDN-PRI transceiver functionality
- Short- and long-haul line interface for clock/data recovery and wave shaping
- CMI coder/decoder
- Crystal-less jitter attenuator
- Dual HDLC controllers
- On-chip programmable BERT generator and detector
- Internal software-selectable receive and transmit side termination resistors
- Dual two-frame elastic-store slip buffers to interface backplanes up to 16.384MHz
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output synthesized to recovered network clock
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- 8-bit parallel control port, multiplexed or nonmultiplexed, Intel or Motorola
- IEEE 1149.1 JTAG-boundary scan
- 3.3V supply with 5V tolerant I/O
- Signaling System 7 (SS7) support

APPLICATIONS:

- Routers
- Channel Service Units (CSUs)
- Data Service Units (DSUs)
- Muxes
- Switches
- Channel Banks
- T1/E1 Test Equipment
- DSL Add/Drop Multiplexers

ORDERING INFORMATION

DS21Q55	27mm BGA	(0°C to +70°C)
DS21Q55N	27mm BGA	(-40°C to +85°C)

1. DESCRIPTION

The DS21Q55 is a quad MCM device featuring independent transceivers that can be software configured for T1, E1, or J1 operation. Each is composed of a line interface unit (LIU), framer, HDLC controllers, and a TDM backplane interface, and is controlled via an 8-bit parallel port configured for Intel or Motorola bus operations. The DS21Q55 is software compatible with the DS2155 single transceiver. It is pin compatible with the DS21Qx5y family of products.

1. DESCRIPTION

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The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary wave shapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX–1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 wave shapes for both 75O coax and 120O twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 43dB or 0dB to 12dB for E1 applications and 0dB to 30dB or 0dB to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths. An additional feature of the LIU is a CMI coder/decoder for interfacing to optical networks.

On the transmit side, clock data and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

Each transceiver has two HDLC controllers. The HDLC controllers transmit and receive data via the framer block. The HDLC controllers can be assigned to any time slot, group of time slots, portion of a time slot or to FDL (T1) or Sa bits (E1). Each controller has a 128-byte transmit FIFO and a 128-byte receive FIFO, thus reducing the amount of processor overhead required to manage the flow of data. In addition, there is built-in support for reducing the processor time required to handle SS7 applications.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow up to eight transceivers (two DS21Q55s) to share a high-speed backplane.

The parallel port provides access for control and configuration of all the DS21Q55's features. The Extended System Information Bus (ESIB) function allows up to eight transceivers, 2 DS21Q55s, to be accessed via a single read for interrupt status or other user selectable alarm status information. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

The device fully meets all of the latest E1 and T1 specifications, including the following:

- ANSI: T1.403-1995, T1.231-1993, T1.408
- AT&T: TR54016, TR62411
- ITU: G.703, G.704, G.706, G.736, G.775, G.823, G.932, I.431, O.151, O.161
- ETSI: ETS 300 011, ETS 300 166, ETS 300 233, CTR4, CTR12
- Japanese: JTG.703, JTI.431, JJ-20.11 (CMI coding only)

1.1 FEATURE HIGHLIGHTS

The DS21Q55 contains all of the features of the previous generation of Dallas Semiconductor's T1 and E1 transceivers plus many new features.

1.1.1 General

- 27mm, 1.27 pitch BGA
- 3.3V supply with 5V tolerant inputs and outputs
- Pin compatible with DS21x5y family
- Software compatible with the DS2155
- Evaluation kits
- IEEE 1149.1 JTAG-boundary scan
- Driver source code available from the factory

1.1.2 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz. Option to use 1.544MHz, 3.088MHz, 6.276MHz, or 12.552MHz for T1-only operation
- Fully software configurable
- Short- and long-haul applications
- Automatic receive sensitivity adjustments
- Ranges include 0dB to -43dB or 0dB to -15dB for E1 applications; 0dB to -36dB or 0dB to -15dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75Ω, 100Ω, and 120Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive-synchronization signal mode
- Flexible transmit-waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- NRZ format option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with exceeded indication of current limit
- Transmit open-circuit-detected indication
- Line interface function can be completely decoupled from the framer/formatter

1.1.3 Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from recovered receive clock

1.1.4 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator

- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

1.1.5 Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive- and transmit-path transparency
- T1 framing formats include D4 (SLC-96) and ESF
- Detailed alarm- and status-reporting with optional interrupt support
- Large path- and line-error counters for:
  - T1 – BPV, CV, CRC6, and framing bit errors
  - E1 – BPV, CV, CRC4, E-bit, and frame alignment errors
  - Timed or manual update modes
- DS1 Idle Code Generation on a per-channel basis in both transmit and receive paths
  - User-defined
  - Digital milliwatt
- ANSI T1.403-1998 support
- E1ETS 300 011 RAI generation
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating-pattern generators and detectors
  - Three independent generators and detectors
  - Patterns from 1 bit to 8 bits or 16 bits in length
- RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state
- Flexible signaling support
  - Software- or hardware-based
  - Interrupt generated on change of signaling data
  - Receive-signaling freeze on loss of sync, carrier loss, or frame slip
- Addition of hardware pins to indicate carrier loss and signaling freeze
- Automatic RAI generation to ETS 300 011 specifications
- Expanded access to Sa and Si bits
- Option to extend carrier-loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
  - Ability to calculate and check CRC6 according to the Japanese standard
  - Ability to generate yellow alarm according to the Japanese standard

1.1.6 System Interface

- Dual two-frame, independent receive and transmit elastic stores
  - Independent control and clocking
    - Controlled-slip capability with status
    - Minimum-delay mode supported
- Maximum 16.384MHz backplane burst rate
- Supports T1 to CEPT (E1) conversion
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation

- Hardware-signaling capability
  - Receive-signaling reinsertion to a backplane, multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- Access to the data streams in between the framer/formatter and the elastic stores
- User-selectable synthesized clock output

1.1.7 HDLC Controllers

- Two independent HDLC controllers
- Fast load and unload features for FIFOs
- SS7 support for FISU transmit and receive
- Independent 128-byte RX and TX buffers with interrupt support
- Access FDL, Sa, or single/multiple DS0 channels
- DS0 access includes Nx64 or Nx56
- Compatible with polled or interrupt-driven environments
- Bit Oriented Code (BOC) support

1.1.8 Test and Diagnostics

- Programmable on-chip Bit Error Rate Testing (BERT)
- Pseudorandom patterns including $QRSS$
- User-defined repetitive patterns
- Daly pattern
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload Error Insertion
- Error insertion in the payload portion of the T1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)

1.1.9 Extended System Information Bus

- Host can read interrupt and alarm status on up to eight ports with a single-bus read

1.1.10 Control Port

- 8-bit parallel control port
- Multiplexed or nonmultiplexed buses
- Intel or Motorola formats
- Supports polled or interrupt-driven environments
- Software access to device ID and silicon revision
- Software-reset supported
  Automatic clear on power-up
- Flexible register-space resets
- Hardware reset pin

Note: This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125µs T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last. The term "locked" is used to refer to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

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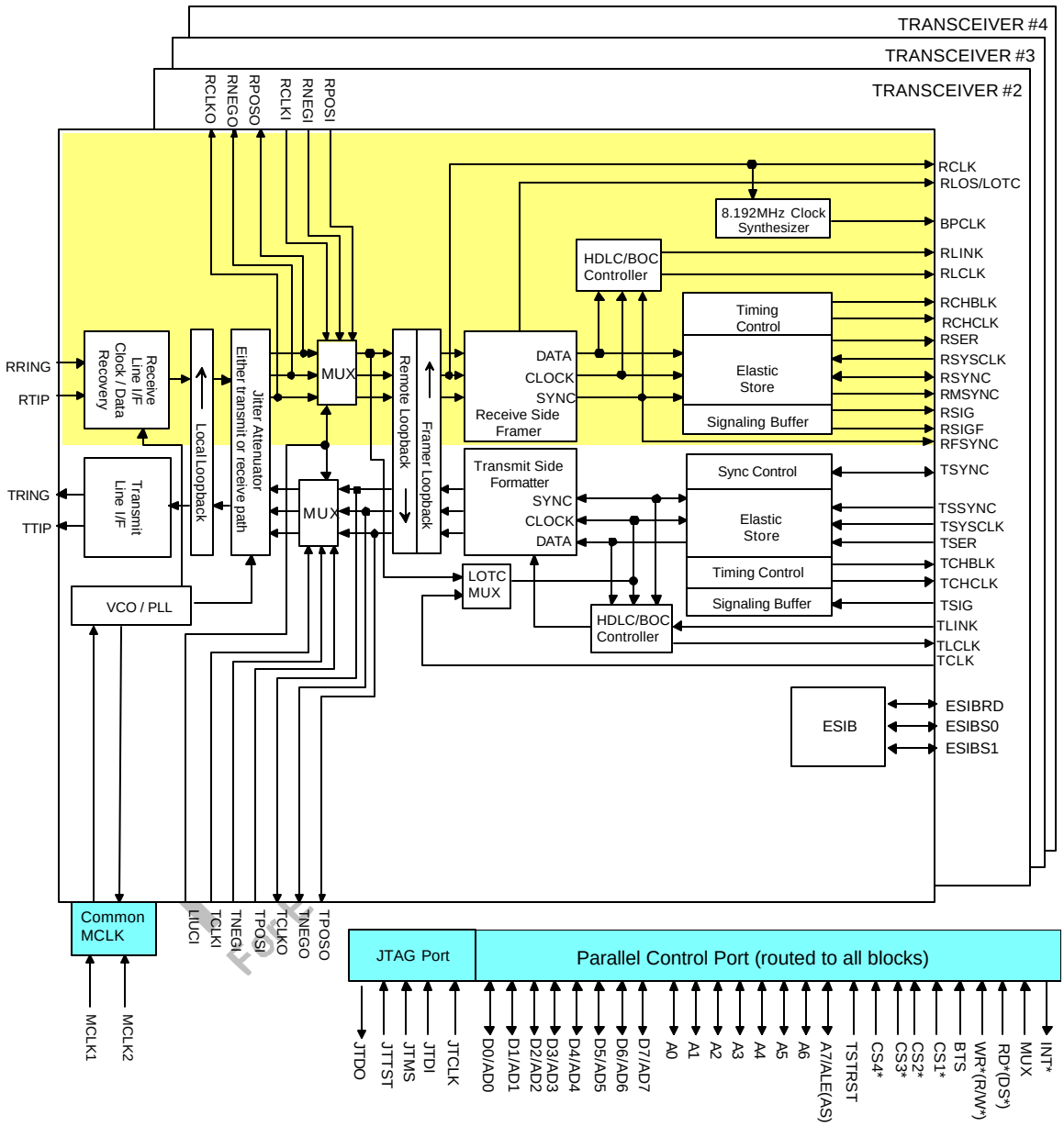
1.2 DOCUMENT REVISION HISTORY

1) Initial Preliminary Release

2. BLOCK DIAGRAM

A simplified block diagram showing the major components of the DS21Q55 is shown in Figure 4-1. Details are shown in subsequent figures. The block diagram is then divided into three functional blocks: LIU, framer, and backplane interface.

BLOCK DIAGRAM Figure 4-1



3. PIN FUNCTION DESCRIPTION

3.1 Transmit Side Pins

Signal Name: **TCLKx**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544 MHz or a 2.048MHz primary clock. Used to clock data through the transmit-side formatter.

Signal Name: **TSERx**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TCHCLKx**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Can also be programmed to output a gated transmit-bit clock for fractional T1/E1 applications. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **TCHBLKx**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the channels. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.

Signal Name: **TSYSCLKx**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic-store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. See *Interleaved PCM Bus Operation* for details on 4.096MHz, 8.192MHz, and 16.384MHz operation using the IBO.

Signal Name: **TLCLKx**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
Demand clock for the transmit link data [TLINK] input.
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **TLINKx**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled, this pin will be sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs-bit position (D4) or the Z–bit position (ZBTSI) or any combination of the Sa bit positions (E1).

Signal Name: **TSYNCx**
Signal Description: **Transmit Sync**
Signal Type: **Input/Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Can be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can also be set via IOCR1.3 to output double-wide pulses at signaling frames in T1 mode.

Signal Name: **TSSYNCx**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit-side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit-side elastic store.

Signal Name: **TSIGx**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TPOSOx**
Signal Description: **Transmit Positive Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data via the output-data format (IOCR1.0)-control bit. This pin is normally tied to TPOSI.

Signal Name: **TNEGOx**
Signal Description: **Transmit Negative Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. This pin is normally tied to TNEGI.

Signal Name: **TCLKOx**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
Buffered clock that is used to clock data through the transmit-side formatter (either TCLK or RCLKI). This pin is normally tied to TCLKI.

Signal Name: **TPOSIx**
Signal Description: **Transmit Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TPOSO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TNEGIx**
Signal Description: **Transmit Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TCLKIx**
Signal Description: **Transmit Clock Input**
Signal Type: **Input**
Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC pin high.

3.2 Receive Side Pins

Signal Name: **RLINKx**
Signal Description: **Receive Link Data**
Signal Type: **Output**
T1 Mode: Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame.
E1 Mode: Updated with the full E1 data stream on the rising edge of RCLK.

Signal Name: **RLCLKx**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock for the RLINK output.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **RCLKx**
Signal Description: **Receive Clock**
Signal Type: **Output**
1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer.

Signal Name: **RCHCLKx**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel can also be programmed to output a gated receive-bit clock for fractional T1/E1 applications. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **RCHBLKx**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See *Channel Blocking Registers*.

Signal Name: **RSERx**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RSYNCx**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (IOCR1.5 = 0) or multiframe (IOCR1.5 = 1) boundaries. If set to output-frame boundaries then via IOCR1.6, RSYNC can also be set to output double-wide pulses on signaling frames in T1 mode. If the receive-side elastic store is enabled, then this pin can be enabled to be an input via IOCR1.4 at which a frame or multiframe boundary pulse is applied.

Signal Name: **RFSYNCx**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8kHz pulse, one RCLK wide, is output at this pin, which identifies frame boundaries.

Signal Name: **RMSYNCx**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
An extracted pulse, one RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), is output at this pin, which identifies multiframe boundaries.

Signal Name: **RSYSCLKx**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, or 8.192MHz clock. Only used when the receive-side elastic-store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. See *Interleaved PCM Bus Operation* for details on 4.096MHz and 8.192MHz operation using the IBO.

Signal Name: **RSIGx**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RLOS/LOTCx**
Signal Description: **Receive Loss of Sync/Loss of Transmit Clock**
Signal Type: **Output**
A dual-function output that is controlled by the CCR1.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µsec.

Signal Name: **RSIGFx**
Signal Description: **Receive Signaling Freeze**
Signal Type: **Output**
Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.

Signal Name: **BPCLKx**
Signal Description: **Back Plane Clock**
Signal Type: **Output**
A user-selectable synthesized clock output that is referenced to the clock that is output at the RCLK pin.

Signal Name: **RPOSOx**
Signal Description: **Receive Positive Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with bipolar data out of the line interface. This pin is normally tied to RPOSI.

Signal Name: **RNEGOx**
Signal Description: **Receive Negative Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RNEGI.

Signal Name: **RCLKOx**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Buffered recovered clock from the network. This pin is normally tied to RCLKI.

Signal Name: **RPOSIx**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC pin high.

Signal Name: **RNEGIx**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC pin high.

Signal Name: **RCLKIx**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive-side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC pin high.

3.3 Parallel Control Port Pins

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during events, alarms, and conditions defined in the status registers. Active-low open-drain output.

Signal Name: **TSTRST**
Signal Description: **3-State Control and Device Reset**
Signal Type: **Input**
A dual-function pin. A zero-to-one transition issues a hardware reset to the DS21Q55 register set. A reset clears all configuration registers. Configuration register contents are set to zero. Leaving TSTRST high will 3-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in-board level testing.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **D0/AD0 to D7/AD7**
Signal Description: **Data Bus [D0 to D7] or Address/Data Bus**
Signal Type: **Input/Output**
In nonmultiplexed bus operation (MUX = 0), it serves as the data bus. In multiplexed bus operation (MUX = 1), it serves as an 8-bit, multiplexed address/data bus.

Signal Name: **A0 to A6**
Signal Description: **Address Bus**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), it serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), A7/ALE(AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: **RD*(DS*)**
Signal Description: **Read Input-Data Strobe**
Signal Type: **Input**
RD* and DS* are active-low signals. DS active HIGH when MUX = 0. See bus timing diagrams.

Signal Name: **CS1***
Signal Description: **Chip Select for transceiver #1**
Signal Type: **Input**
Must be low to read or write to transceiver #1 of the device. CS1* is an active-low signal.

Signal Name: **CS2***
Signal Description: **Chip Select for transceiver #2**
Signal Type: **Input**
Must be low to read or write to transceiver #2 of the device. CS2* is an active-low signal.

Signal Name: **CS3***
Signal Description: **Chip Select for transceiver #3**
Signal Type: **Input**
Must be low to read or write to transceiver #3 of the device. CS3* is an active-low signal.

Signal Name: **CS4***
Signal Description: **Chip Select for transceiver #4**
Signal Type: **Input**
Must be low to read or write to transceiver #4 of the device. CS4* is an active-low signal.

Signal Name: **A7/ALE(AS)**
Signal Description: **A7 or Address Latch Enable(Address Strobe)**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), it serves as the upper address bit. In multiplexed bus operation (MUX = 1), it serves to demultiplex the bus on a positive-going edge.

Signal Name: **WR*(R/W*)**
Signal Description: **Write Input(Read/Write)**
Signal Type: **Input**
WR* is an active-low signal.

3.4 Extended System Information Bus

Signal Name: **ESIBS0x**
Signal Description: **Extended System Information Bus Select 0**
Signal Type: **Input/Output**
Used to group two DS21Q55s into a bus-sharing mode for alarm and status reporting. See *Extended System Information Bus (ESIB)* for more details.

Signal Name: **ESIBS1x**
Signal Description: **Extended System Information Bus Select 1**
Signal Type: **Input/Output**
Used to group two DS21Q55s into a bus-sharing mode for alarm and status reporting. See *Extended System Information Bus (ESIB)* for more details.

Signal Name: **ESIBRDx**
Signal Description: **Extended System Information Bus Read**
Signal Type: **Input/Output**
Used to group two DS21Q55s into a bus-sharing mode for alarm and status reporting. See *Extended System Information Bus (ESIB)* for more details.

3.5 JTAG Test Access Port Pins

Signal Name: **JTRST**
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
JTRST is used to asynchronously reset the test access port controller. After power-up, JTRST must be toggled fromlow to high. This action will set the device into the JTAG DEVICE ID mode. Normal device operation is restored by pulling JTRST low. JTRST is pulled HIGH internally via a 10k resistor operation.

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test-access port into the various defined IEEE 1149.1 states. This pin has a 10k pullup resistor.

Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.

Signal Name: **JTDI**
Signal Description: **IEEE 1149.1 Test Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10k pullup resistor.

Signal Name: **JTDO**
Signal Description: **IEEE 1149.1 Test Data Output**
Signal Type: **Output**
Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.

3.6 Line Interface Pins

Signal Name: **MCLK1**
Signal Description: **Master Clock Input for Transceivers 1 & 2**
Signal Type: **Input**
A (50ppm) clock source. This clock is used internally for both clock/data recovery and for the jitter attenuator for both T1 and E1 modes. A quartz crystal of 2.048MHz can be applied across MCLK and XTALD instead of the clock source. The clock rate can be 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz. When using the DS21Q55 in T1-only operation a 1.544MHz (50ppm) clock source can be used. MCLK1 and MCLK2 may be driven from a common clock.

Signal Name: **MCLK2**
Signal Description: **Master Clock Input for Transceivers 3 & 4**
Signal Type: **Input**
A (50ppm) clock source. This clock is used internally for both clock/data recovery and for the jitter attenuator for both T1 and E1 modes. A quartz crystal of 2.048MHz can be applied across MCLK and XTALD instead of the clock source. The clock rate can be 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz. When using the DS21Q55 in T1-only operation a 1.544MHz (50ppm) clock source can be used. MCLK1 and MCLK2 may be driven from a common clock.

Signal Name: **LIUC**
Signal Description: **Line Interface Connect**
Signal Type: **Input**
Tie low to separate the line interface circuitry from the framer/formatter circuitry and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. Tie high to connect the line interface circuitry to the framer/formatter circuitry and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. When LIUC is tied high, the TPOSI/TNEGI/TCLKI/ RPOSI/RNEGI/RCLKI pins should be tied low.

Signal Name: **RTIPx and RRINGx**
Signal Description: **Receive Tip and Ring**
Signal Type: **Input**
Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See *Line Interface Unit* for details.

Signal Name: **TTIPx and TRINGx**
Signal Description: **Transmit Tip and Ring**
Signal Type: **Output**
Analog line driver outputs. These pins connect via a 1:2 step-up transformer to the network. See *Line Interface Unit* for details.

3.7 Supply Pins

Signal Name: **DV_{DD}**
Signal Description: **Digital Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the RV_{DD} and TV_{DD} pins.

Signal Name: **RV_{DD}**
Signal Description: **Receive Analog Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the DV_{DD} and TV_{DD} pins.

Signal Name: **TV_{DD}**
Signal Description: **Transmit Analog Positive Supply**
Signal Type: **Supply**
3.3V ±5% Should be tied to the RV_{DD} and DV_{DD} pins.

Signal Name: **DV_{SS}**
Signal Description: **Digital Signal Ground**
Signal Type: **Supply**
Should be tied to the RV_{SS} and TV_{SS} pins.

Signal Name: **RV_{SS}**
Signal Description: **Receive Analog Signal Ground**
Signal Type: **Supply**
0.0V. Should be tied to DV_{SS} and TV_{SS}.

Signal Name: **TV_{SS}**
Signal Description: **Transmit Analog Signal Ground**
Signal Type: **Supply**
0.0V. Should be tied to DV_{SS} and RV_{SS}.

3.8 Pinout

DS21Q55 PIN DESCRIPTION Table 5-1

NOTE: Signal is common to all transceivers unless otherwise stated

PIN	SYMBOL	TYPE	DESCRIPTION
U3	A0	I	Address Bus Bit 0 (lsb).
L17	A1	I	Address Bus Bit 1.
V2	A2	I	Address Bus Bit 2.
T4	A3	I	Address Bus Bit 3.
V8	A4	I	Address Bus Bit 4.
H4	A5	I	Address Bus Bit 5.
U8	A6	I	Address Bus Bit 6.
P4	A7/ALE(AS)	I	Address Bus Bit 7 (msb) / Address Latch Enable.
M1	BPCLK1	O	Back Plane Clock, Transceiver # 1.
H17	BPCLK2	O	Back Plane Clock, Transceiver # 2.
F4	BPCLK3	O	Back Plane Clock, Transceiver # 3.
V13	BPCLK4	O	Back Plane Clock, Transceiver # 4.
P2	BTS	I	Bus Type Select (0 = Intel / 1 = Motorola),
P3	CS1*	I	Chip Select, Transceiver # 1.
A14	CS2*	I	Chip Select, Transceiver # 2.
B5	CS3*	I	Chip Select, Transceiver # 3.
K17	CS4*	I	Chip Select, Transceiver # 4.
U11	D0/AD0	I/O	Data Bus Bit 0/ Address/Data Bus Bit 0 (lsb).
J19	D1/AD1	I/O	Data Bus Bit 1/ Address/Data Bus Bit 1.
W15	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus Bit 2.
U7	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3.
U9	D4/AD4	I/O	Data Bus Bit 4/Address/Data Bus Bit 4.
U5	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5.
V4	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6.
U4	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7 (msb).
J3	DVDD1	–	Digital Positive Supply.
N4	DVDD1	–	Digital Positive Supply.
U2	DVDD1	–	Digital Positive Supply.
V5	DVDD1	–	Digital Positive Supply.
B12	DVDD2	–	Digital Positive Supply.
C12	DVDD2	–	Digital Positive Supply.
C16	DVDD2	–	Digital Positive Supply.
D18	DVDD2	–	Digital Positive Supply.
A9	DVDD3	–	Digital Positive Supply.
B3	DVDD3	–	Digital Positive Supply.
B6	DVDD3	–	Digital Positive Supply.
C4	DVDD3	–	Digital Positive Supply.
G20	DVDD4	–	Digital Positive Supply.
M17	DVDD4	–	Digital Positive Supply.
M20	DVDD4	–	Digital Positive Supply.
P18	DVDD4	–	Digital Positive Supply.
H3	DVSS1	–	Digital Signal Ground.
U6	DVSS1	–	Digital Signal Ground.
W8	DVSS1	–	Digital Signal Ground.
A17	DVSS2	–	Digital Signal Ground.

PIN	SYMBOL	TYPE	DESCRIPTION
A20	DVSS2	–	Digital Signal Ground.
B11	DVSS2	–	Digital Signal Ground.
A5	DVSS3	–	Digital Signal Ground.
B7	DVSS3	–	Digital Signal Ground.
B9	DVSS3	–	Digital Signal Ground.
H20	DVSS4	–	Digital Signal Ground
L20	DVSS4	–	Digital Signal Ground
N17	DVSS4	–	Digital Signal Ground
J4	ESIBRD1	–	Extended System Information Bus Read, Transceiver # 1.
C13	ESIBRD2	–	Extended System Information Bus Read, Transceiver # 2.
C3	ESIBRD3	–	Extended System Information Bus Read, Transceiver # 3.
U13	ESIBRD4	–	Extended System Information Bus Read, Transceiver # 4.
W6	ESIBS0_1	I/O	Extended System Information Bus 0, Transceiver # 1.
F18	ESIBS0_2	I/O	Extended System Information Bus 0, Transceiver # 2.
D7	ESIBS0_3	I/O	Extended System Information Bus 0, Transceiver # 3.
T20	ESIBS0_4	I/O	Extended System Information Bus 0, Transceiver # 4.
V9	ESIBS1_1	I/O	Extended System Information Bus 1, Transceiver # 1.
B17	ESIBS1_2	I/O	Extended System Information Bus 1, Transceiver # 2.
A6	ESIBS1_3	I/O	Extended System Information Bus 1, Transceiver # 3.
J20	ESIBS1_4	I/O	Extended System Information Bus 1, Transceiver # 4.
U1	INT*	O	Interrupt.
Y15	JTCLK	I	JTAG Clock.
N1	JTDI	I	JTAG Data Input, Transceiver #1
V19	JTDO	O	JTAG Data Output. Transceiver #4
W13	JTMS	I	JTAG Test Mode Select.
V18	JTRST*	I	JTAG Reset.
K2	LIUC	I	Line Interface Connect.
T1	MCLK1	I	Master Clock, Transceiver #1 and, Transceiver #3.
W20	MCLK2	I	Master Clock, Transceiver #2 and, Transceiver #4.
U10	MUX	I	Mux Bus Select.
M2	RCHBLK1	O	Receive Channel Block, Transceiver #1.
G17	RCHBLK2	O	Receive Channel Block, Transceiver #2.
G4	RCHBLK3	O	Receive Channel Block, Transceiver #3.
Y12	RCHBLK4	O	Receive Channel Block, Transceiver #4.
J1	RCHCLK1	O	Receive Channel Clock, Transceiver #1.
D14	RCHCLK2	O	Receive Channel Clock, Transceiver #2.
F3	RCHCLK3	O	Receive Channel Clock, Transceiver #3.
U14	RCHCLK4	O	Receive Channel Clock, Transceiver #4.
N3	RCLK1	O	Receive Clock Output from the Framer, Transceiver #1.
B13	RCLK2	O	Receive Clock Output from the Framer, Transceiver #2.
E3	RCLK3	O	Receive Clock Output from the Framer, Transceiver #3.
M18	RCLK4	O	Receive Clock Output from the Framer, Transceiver #4.
M4	RCLKI1	I	Receive Clock Input for the LIU, Transceiver #1.
A15	RCLKI2	I	Receive Clock Input for the LIU, Transceiver #2.
A4	RCLKI3	I	Receive Clock Input for the LIU, Transceiver #3.
R17	RCLKI4	I	Receive Clock Input for the LIU, Transceiver #4.
M3	RCLKO1	O	Receive Clock Output from the LIU, Transceiver #1.
C14	RCLKO2	O	Receive Clock Output from the LIU, Transceiver #2.
B4	RCLKO3	O	Receive Clock Output from the LIU, Transceiver #3.
T17	RCLKO4	O	Receive Clock Output from the LIU, Transceiver #4.
N2	RD*(DS*)	I	Read Input (Data Strobe)
K4	RFSYNC1	O	Receive Frame Sync (before the receive elastic store), Transceiver

PIN	SYMBOL	TYPE	DESCRIPTION
			#1.
D17	RFSYNC2	O	Receive Frame Sync (before the receive elastic store), Transceiver #2.
A2	RFSYNC3	O	Receive Frame Sync (before the receive elastic store), Transceiver #3.
V14	RFSYNC4	O	Receive Frame Sync (before the receive elastic store), Transceiver #4.
F1	RLCLK1	O	Receive Link Clock, Transceiver #1.
A12	RLCLK2	O	Receive Link Clock, Transceiver #2.
D3	RLCLK3	O	Receive Link Clock, Transceiver #3.
K18	RLCLK4	O	Receive Link Clock, Transceiver #4.
G2	RLINK1	O	Receive Link Data, Transceiver #1.
A13	RLINK2	O	Receive Link Data, Transceiver #2.
A3	RLINK3	O	Receive Link Data, Transceiver #3.
U12	RLINK4	O	Receive Link Data, Transceiver #4.
H2	RLOS/LOTC1	O	Receive Loss Of Sync / Loss Of Transmit Clock, Transceiver #1.
E17	RLOS/LOTC2	O	Receive Loss Of Sync / Loss Of Transmit Clock, Transceiver #2.
E1	RLOS/LOTC3	O	Receive Loss Of Sync / Loss Of Transmit Clock, Transceiver #3.
V11	RLOS/LOTC4	O	Receive Loss Of Sync / Loss Of Transmit Clock, Transceiver #4.
L1	RMSYNC1	O	Receive Multiframe Sync, Transceiver #1.
D16	RMSYNC2	O	Receive Multiframe Sync, Transceiver #2.
F2	RMSYNC3	O	Receive Multiframe Sync, Transceiver #3.
W16	RMSYNC4	O	Receive Multiframe Sync, Transceiver #4.
R3	RNEGI1	I	Receive Negative Data for the Framer, Transceiver #1.
D13	RNEGI2	I	Receive Negative Data for the Framer, Transceiver #2.
A1	RNEGI3	I	Receive Negative Data for the Framer, Transceiver #3.
P17	RNEGI4	I	Receive Negative Data for the Framer, Transceiver #4.
L3	RNEGO1	O	Receive Negative Data from the LIU, Transceiver #1.
B15	RNEGO2	O	Receive Negative Data from the LIU, Transceiver #2.
C2	RNEGO3	O	Receive Negative Data from the LIU, Transceiver #3.
U17	RNEGO4	O	Receive Negative Data from the LIU, Transceiver #4.
R4	RPOSI1	I	Receive Positive Data for the Framer, Transceiver #1.
B14	RPOSI2	I	Receive Positive Data for the Framer, Transceiver #2.
B2	RPOSI3	I	Receive Positive Data for the Framer, Transceiver #3.
V15	RPOSI4	I	Receive Positive Data for the Framer, Transceiver #4.
L4	RPOSO1	O	Receive Positive Data from the LIU, Transceiver #1.
A16	RPOSO2	O	Receive Positive Data from the LIU, Transceiver #2.
B1	RPOSO3	O	Receive Positive Data from the LIU, Transceiver #3.
U15	RPOSO4	O	Receive Positive Data from the LIU, Transceiver #4.
Y11	RRING1	I	Receive Analog Ring Input, Transceiver #1.
Y14	RRING2	I	Receive Analog Ring Input, Transceiver #2.
Y17	RRING3	I	Receive Analog Ring Input, Transceiver #3.
Y20	RRING4	I	Receive Analog Ring Input, Transceiver #4.
J2	RSER1	O	Receive Serial Data, Transceiver #1.
D15	RSER2	O	Receive Serial Data, Transceiver #2.
E2	RSER3	O	Receive Serial Data, Transceiver #3.
W17	RSER4	O	Receive Serial Data, Transceiver #4.
L2	RSIG1	O	Receive Signaling Output, Transceiver #1.
B16	RSIG2	O	Receive Signaling Output, Transceiver #2.
C1	RSIG3	O	Receive Signaling Output, Transceiver #3.
Y18	RSIG4	O	Receive Signaling Output, Transceiver #4.
K1	RSIGF1	O	Receive Signaling Freeze Output, Transceiver #1.
C15	RSIGF2	O	Receive Signaling Freeze Output, Transceiver #2.

PIN	SYMBOL	TYPE	DESCRIPTION
D2	RSIGF3	O	Receive Signaling Freeze Output, Transceiver #3.
V16	RSIGF4	O	Receive Signaling Freeze Output, Transceiver #4.
G1	RSYNC1	I/O	Receive Sync, Transceiver #1.
D12	RSYNC2	I/O	Receive Sync, Transceiver #2.
D1	RSYNC3	I/O	Receive Sync, Transceiver #3.
V12	RSYNC4	I/O	Receive Sync, Transceiver #4.
H1	RSYSCLK1	I	Receive System Clock, Transceiver #1.
F17	RSYSCLK2	I	Receive System Clock, Transceiver #2.
G3	RSYSCLK3	I	Receive System Clock, Transceiver #3.
W14	RSYSCLK4	I	Receive System Clock, Transceiver #4.
Y10	RTIP1	I	Receive Analog Tip Input, Transceiver #1.
Y13	RTIP2	I	Receive Analog Tip Input, Transceiver #2.
Y16	RTIP3	I	Receive Analog Tip Input, Transceiver #3.
Y19	RTIP4	I	Receive Analog Tip Input, Transceiver #4.
P1	RVDD1	–	Receive Analog Positive Supply.
J17	RVDD2	–	Receive Analog Positive Supply.
E4	RVDD3	–	Receive Analog Positive Supply.
W18	RVDD4	–	Receive Analog Positive Supply.
R2	RVSS1	–	Receive Analog Signal Ground
T2	RVSS1	–	Receive Analog Signal Ground
H19	RVSS2	–	Receive Analog Signal Ground
J18	RVSS2	–	Receive Analog Signal Ground
D4	RVSS3	–	Receive Analog Signal Ground
D5	RVSS3	–	Receive Analog Signal Ground
V20	RVSS4	–	Receive Analog Signal Ground
W19	RVSS4	–	Receive Analog Signal Ground
W1	TCHBLK1	O	Transmit Channel Block, Transceiver #1.
F20	TCHBLK2	O	Transmit Channel Block, Transceiver #2.
C11	TCHBLK3	O	Transmit Channel Block, Transceiver #3.
U20	TCHBLK4	O	Transmit Channel Block, Transceiver #4.
V10	TCHCLK1	O	Transmit Channel Clock, Transceiver #1.
A18	TCHCLK2	O	Transmit Channel Clock, Transceiver #2.
B8	TCHCLK3	O	Transmit Channel Clock, Transceiver #3.
L18	TCHCLK4	O	Transmit Channel Clock, Transceiver #4.
Y9	TCLK1	I	Transmit Clock, Transceiver #1.
B19	TCLK2	I	Transmit Clock, Transceiver #2.
B10	TCLK3	I	Transmit Clock, Transceiver #3.
M19	TCLK4	I	Transmit Clock, Transceiver #4.
V6	TCLKI1	I	Transmit Clock Input for the LIU, Transceiver #1.
D19	TCLKI2	I	Transmit Clock Input for the LIU, Transceiver #2.
C8	TCLKI3	I	Transmit Clock Input for the LIU, Transceiver #3.
P20	TCLKI4	I	Transmit Clock Input for the LIU, Transceiver #4.
W7	TCLKO1	O	Transmit Clock Output from the Framer, Transceiver #1.
E18	TCLKO2	O	Transmit Clock Output from the Framer, Transceiver #2.
A7	TCLKO3	O	Transmit Clock Output from the Framer, Transceiver #3.
P19	TCLKO4	O	Transmit Clock Output from the Framer, Transceiver #4.
V3	TLCLK1	O	Transmit Link Clock, Transceiver #1.
E20	TLCLK2	O	Transmit Link Clock, Transceiver #2.
D6	TLCLK3	O	Transmit Link Clock, Transceiver #3.
T18	TLCLK4	O	Transmit Link Clock, Transceiver #4.
W5	TLINK1	I	Transmit Link Data, Transceiver #1.
E19	TLINK2	I	Transmit Link Data, Transceiver #2.

PIN	SYMBOL	TYPE	DESCRIPTION
C6	TLINK3	I	Transmit Link Data, Transceiver #3.
T19	TLINK4	I	Transmit Link Data, Transceiver #4.
R1	TNEGI1	I	Transmit Negative Data Input for the LIU, Transceiver #1.
F19	TNEGI2	I	Transmit Negative Data Input for the LIU, Transceiver #2.
D8	TNEGI3	I	Transmit Negative Data Input for the LIU, Transceiver #3.
R20	TNEGI4	I	Transmit Negative Data Input for the LIU, Transceiver #4.
T3	TNEGO1	O	Transmit Negative Data Output from Framer, Transceiver #1.
B20	TNEGO2	O	Transmit Negative Data Output from Framer, Transceiver #2.
D9	TNEGO3	O	Transmit Negative Data Output from Framer, Transceiver #3.
N20	TNEGO4	O	Transmit Negative Data Output from Framer, Transceiver #4.
W3	TPOSI1	I	Transmit Positive Data Input for the LIU, Transceiver #1.
C20	TPOSI2	I	Transmit Positive Data Input for the LIU, Transceiver #2.
A8	TPOSI3	I	Transmit Positive Data Input for the LIU, Transceiver #3.
R19	TPOSI4	I	Transmit Positive Data Input for the LIU, Transceiver #4.
V7	TPOSO1	O	Transmit Positive Data Output from Framer, Transceiver #1.
C19	TPOSO2	O	Transmit Positive Data Output from Framer, Transceiver #2.
C9	TPOSO3	O	Transmit Positive Data Output from Framer, Transceiver #3.
N19	TPOSO4	O	Transmit Positive Data Output from Framer, Transceiver #4.
Y2	TRING1	O	Transmit Analog Ring Output, Transceiver #1.
Y4	TRING2	O	Transmit Analog Ring Output, Transceiver #2.
Y6	TRING3	O	Transmit Analog Ring Output, Transceiver #3.
Y8	TRING4	O	Transmit Analog Ring Output, Transceiver #4.
W9	TSER1	I	Transmit Serial Data, Transceiver #1.
C17	TSER2	I	Transmit Serial Data, Transceiver #2.
C10	TSER3	I	Transmit Serial Data, Transceiver #3.
K20	TSER4	I	Transmit Serial Data, Transceiver #4.
W10	TSIG1	I	Transmit Signaling Input, Transceiver #1.
C18	TSIG2	I	Transmit Signaling Input, Transceiver #2.
A10	TSIG3	I	Transmit Signaling Input, Transceiver #3.
L19	TSIG4	I	Transmit Signaling Input, Transceiver #4.
W12	TSSYNC1	I	Transmit System Sync, Transceiver #1.
B18	TSSYNC2	I	Transmit System Sync, Transceiver #2.
D10	TSSYNC3	I	Transmit System Sync, Transceiver #3.
K19	TSSYNC4	I	Transmit System Sync, Transceiver #4.
U16	TSTRST	I	Test/Reset
V1	TSYNC1	I/O	Transmit Sync, Transceiver #1.
D20	TSYNC2	I/O	Transmit Sync, Transceiver #2.
C7	TSYNC3	I/O	Transmit Sync, Transceiver #3.
R18	TSYNC4	I/O	Transmit Sync, Transceiver #4.
W11	TSYSCLK1	I	Transmit System Clock, Transceiver #1.
A19	TSYSCLK2	I	Transmit System Clock, Transceiver #2.
A11	TSYSCLK3	I	Transmit System Clock, Transceiver #3.
N18	TSYSCLK4	I	Transmit System Clock, Transceiver #4.
Y1	TTIP1	O	Transmit Analog Tip Output, Transceiver #1.
Y3	TTIP2	O	Transmit Analog Tip Output, Transceiver #2.
Y5	TTIP3	O	Transmit Analog Tip Output, Transceiver #3.
Y7	TTIP4	O	Transmit Analog Tip Output, Transceiver #4.
W2	TVDD1	–	Transmit Analog Positive Supply.
G19	TVDD2	–	Transmit Analog Positive Supply.
D11	TVDD3	–	Transmit Analog Positive Supply.
U19	TVDD4	–	Transmit Analog Positive Supply.
W4	TVSS1	–	Transmit Analog Signal Ground.

PIN	SYMBOL	TYPE	DESCRIPTION
G18	TVSS2	–	Transmit Analog Signal Ground.
C5	TVSS3	–	Transmit Analog Signal Ground.
U18	TVSS4	–	Transmit Analog Signal Ground.
K3	WR* (R/W*)	I	Write Input (Read/Write).

3.9 Package

DS21Q55 Pin DIAGRAM, 27mm BGA Figure 5-1

The diagram shown below is the lead pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rnegi 3	rfsync 3	rlink 3	rclki 3	dvss 3	esibs1 3	tclko 3	tposi 3	dvdd 3	tsig 3	tsysclk 3	rlclk 2	rlink 2	cs 2*	rclki 2	rposo 2	dvss 2	tchclk 2	tsysclk 2	dvss 2
B	rposo 3	rposi 3	dvdd 3	rclko 3	cs 3*	dvdd 3	dvss 3	tchclk 3	dvss 3	tclk 3	dvss 2	dvdd 2	rclk 2	rposi 2	rnego 2	rsig 2	esibs1 2	tssync 2	tclk 2	tnego 2
C	rsig 3	rnego 3	eisbrd 3	dvdd 3	tvss 3	tlink 3	tsync 3	tclki 3	tposo 3	tser 3	tchblk 3	dvdd 2	eisbrd 2	rclko 2	rsigf 2	dvdd 2	tser 2	tsig 2	tposo 2	tposi 2
D	rsync 3	rsigf 3	rlclk 3	rvss 3	rvss 3	tlclk 3	esibs0 3	tnegi 3	tnego 3	tssync 3	tvdd 3	rsync 2	rnegi 2	rchclk 2	rser 2	rmsync 2	rfsync 2	dvdd 2	tclki 2	tsync 2
E	rlos 3	rser 3	rclk 3	rvdd 3													rlos 2	tclko 2	tlink 2	tlclk 2
F	rlclk 1	rmsync 3	rchclk 3	bpclk 3													rsysclk 2	esibs0 2	tnegi 2	tchblk 2
G	rsync 1	rlink 1	rsysclk 3	rchblk 3													rchblk 2	tvss 2	tvdd 2	dvdd 4
H	rsysclk 1	rlos 1	dvss 1	a5													bpclk 2	NC	rvss 2	dvss 4
J	rchclk 1	rser 1	dvdd 1	eisbrd 1													rvdd 2	rvss 2	D1/ AD1	esibs1 4
K	rsigf 1	liuc	wr*	rfsync 1													cs 4*	rlclk 4	tssync 4	tser 4
L	rmsync 1	rsig 1	rnego 1	rposo 1													A1	tchclk 4	tsig 4	dvss 4
M	bpclk 1	rchblk 1	rclko 1	rclki 1													dvdd 4	rclk 4	tclk 4	dvdd 4
N	jtdi	rd*	rclk 1	dvdd 1													dvss 4	tsys clk4	tposo 4	tnego 4
P	rvdd 1	bts	cs 1*	A7/ALE(AS)													rnegi 4	dvdd 4	tclko 4	tclki 4
R	tnegi 1	rvss 1	rnegi 1	rposi 1													rclki 4	tsync 4	tposi 4	tnegi 4
T	mclk 1	rvss 1	tnego 1	A3													rclko 4	tlclk 4	tlink 4	esibs0 4
U	int*	dvdd 1	A0	D7/ AD7	D5/ AD5	dvss 1	D3/ AD3	A6	D4/ AD4	mux	D0/ AD0	rlink 4	eisbrd 4	rchclk 4	rposo 4	tstrst	rnego 4	tvss 4	tvdd 4	tchblk 4
V	tsync 1	A2	tlclk 1	D6/ AD6	dvdd 1	tclki 1	tposo 1	A4	esibs1 1	tchclk 1	rlos 4	rsync 4	bpclk 4	rfsync 4	rposi 4	rsigf 4	NC	jtrst*	jtdo	rvss 4
W	tchblk 1	tvdd 1	tposi 1	tvss 1	tlink 1	esibs0 1	tclko 1	dvss 1	tser 1	tsig 1	tsysclk 1	tssync 1	jtms	rsysclk 4	D2/ AD2	rmsync 4	rser 4	rvdd 4	rvss 4	mclk 2
Y	ttip 1	tring 1	ttip 2	tring 2	ttip 3	tring 3	ttip 4	tring 4	tclk 1	rtip 1	rring 1	rchblk 4	rtip 2	rring 2	jtclk	rtip 3	rring 3	rsig 4	rtip 4	rring 4

NOTE: Locations C3, C13, J4, and U13 are used for the Extended System Information Bus (ESIB). These pin locations on the DS21Q352, DS21Q354, DS21Q552, and DS21Q554 are connected to ground. When replacing a DS21Qx5y with a DS21Q55B, these signals should be routed to control logic in order to gain access to the ESIB. If these pins remain connected to ground, the ESIB function will be disabled.

4. PARALLEL PORT

The DS21Q55 is controlled via a nonmultiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The DS21Q55 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the *AC Electrical Characteristics* for more details. Each of the four transceivers has a complete register set as shown below. There are four individual Chip Select signals (CS1*, CS2*, CS3*, CS4*) that are used select one of the four transceivers.

4.1 Register Map

REGISTER MAP SORTED BY ADDRESS ***Table 6-1***

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION	PAGE
00		**MASTER MODE REGISTER**	MSTRREG	*
01		I/O Configuration Register 1	IOCR1	*
02		I/O Configuration Register 2	IOCR2	*
03		T1 Receive Control Register 1	T1RCR1	*
04		T1 Receive Control Register 2	T1RCR2	*
05		T1 Transmit Control Register 1	T1TCR1	*
06		T1 Transmit Control Register 2	T1TCR2	*
07		T1 Common Control Register 1	T1CCR1	*
08		Software Signaling Insertion Enable 1	SSIE1	*
09		Software Signaling Insertion Enable 2	SSIE2	*
0A		Software Signaling Insertion Enable 3	SSIE3	*
0B		Software Signaling Insertion Enable 4	SSIE4	*
0C		T1 Receive Digital Milliwatt Enable Register 1	T1RDMR1	*
0D		T1 Receive Digital Milliwatt Enable Register 2	T1RDMR2	*
0E		T1 Receive Digital Milliwatt Enable Register 3	T1RDMR3	*
0F		Device Identification Register	IDR	*
10		Information Register 1	INFO1	*
11		Information Register 2	INFO2	*
12		Information Register 3	INFO3	*
13		Test Register	TEST	*
14		Interrupt Information Register 1	IIR1	*
15		Interrupt Information Register 2	IIR2	*
16		Status Register 1	SR1	*
17		Interrupt Mask Register 1	IMR1	*
18		Status Register 2	SR2	*
19		Interrupt Mask Register 2	IMR2	*
1A		Status Register 3	SR3	*
1B		Interrupt Mask Register 3	IMR3	*
1C		Status Register 4	SR4	*
1D		Interrupt Mask Register 4	IMR4	*
1E		Status Register 5	SR5	*
1F		Interrupt Mask Register 5	IMR5	*
20		Status Register 6	SR6	*
21		Interrupt Mask Register 6	IMR6	*
22		Status Register 7	SR7	*
23		Interrupt Mask Register 7	IMR7	*
24		Status Register 8	SR8	*
25		Interrupt Mask Register 8	IMR8	*

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION	PAGE
26		Status Register 9	SR9	*
27		Interrupt Mask Register 9	IMR9	*
28		Per-Channel Pointer Register	PCPR	*
29		Per-Channel Data Register 1	PCDR1	*
2A		Per-Channel Data Register 2	PCDR2	*
2B		Per-Channel Data Register 3	PCDR3	*
2C		Per-Channel Data Register 4	PCDR4	*
2D		Information Register 4	INFO4	*
2E		Information Register 5	INFO5	*
2F		Information Register 6	INFO6	*
30		Information Register 7	INFO7	*
31		HDLC #1 Receive Control	H1RC	*
32		HDLC #2 Receive Control	H2RC	*
33		E1 Receive Control Register 1	E1RCR1	*
34		E1 Receive Control Register 2	E1RCR2	*
35		E1 Transmit Control Register 1	E1TCR1	*
36		E1 Transmit Control Register 2	E1TCR2	*
37		BOC Control Register	BOCC	*
38		Receive Signaling Change Of State Information 1	RSINFO1	*
39		Receive Signaling Change Of State Information 2	RSINFO2	*
3A		Receive Signaling Change Of State Information 3	RSINFO3	*
3B		Receive Signaling Change Of State Information 4	RSINFO4	*
3C		Receive Signaling Change Of State Interrupt Enable 1	RSCSE1	*
3D		Receive Signaling Change Of State Interrupt Enable 2	RSCSE2	*
3E		Receive Signaling Change Of State Interrupt Enable 3	RSCSE3	*
3F		Receive Signaling Change Of State Interrupt Enable 4	RSCSE4	*
40		Signaling Control Register	SIGCR	*
41		Error Count Configuration Register	ERCNT	*
42		Line Code Violation Count Register 1	LCVCR1	*
43		Line Code Violation Count Register 2	LCVCR2	*
44		Path Code Violation Count Register 1	PCVCR1	*
45		Path Code Violation Count Register 2	PCVCR2	*
46		Frames Out of Sync Count Register 1	FOSCR1	*
47		Frames Out of Sync Count Register 2	FOSCR2	*
48		E-Bit Count Register 1	EBCR1	*
49		E-Bit Count Register 2	EBCR2	*
4A		Loopback Control Register	LBCR	*
4B		Per-Channel Loopback Enable Register 1	PCLR1	*
4C		Per-Channel Loopback Enable Register 2	PCLR2	*
4D		Per-Channel Loopback Enable Register 3	PCLR3	*
4E		Per-Channel Loopback Enable Register 4	PCLR4	*
4F		Elastic Store Control Register	ESCR	*
50		Transmit Signaling Register 1	TS1	*
51		Transmit Signaling Register 2	TS2	*
52		Transmit Signaling Register 3	TS3	*
53		Transmit Signaling Register 4	TS4	*
54		Transmit Signaling Register 5	TS5	*
55		Transmit Signaling Register 6	TS6	*
56		Transmit Signaling Register 7	TS7	*
57		Transmit Signaling Register 8	TS8	*
58		Transmit Signaling Register 9	TS9	*
59		Transmit Signaling Register 10	TS10	*

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION	PAGE
5A		Transmit Signaling Register 11	TS11	*
5B		Transmit Signaling Register 12	TS12	*
5C		Transmit Signaling Register 13	TS13	*
5D		Transmit Signaling Register 14	TS14	*
5E		Transmit Signaling Register 15	TS15	*
5F		Transmit Signaling Register 16	TS16	*
60		Receive Signaling Register 1	RS1	*
61		Receive Signaling Register 2	RS2	*
62		Receive Signaling Register 3	RS3	*
63		Receive Signaling Register 4	RS4	*
64		Receive Signaling Register 5	RS5	*
65		Receive Signaling Register 6	RS6	*
66		Receive Signaling Register 7	RS7	*
67		Receive Signaling Register 8	RS8	*
68		Receive Signaling Register 9	RS9	*
69		Receive Signaling Register 10	RS10	*
6A		Receive Signaling Register 11	RS11	*
6B		Receive Signaling Register 12	RS12	*
6C		Receive Signaling Register 13	RS13	*
6D		Receive Signaling Register 14	RS14	*
6E		Receive Signaling Register 15	RS15	*
6F		Receive Signaling Register 16	RS16	*
70		Common Control Register 1	CCR1	*
71		Common Control Register 2	CCR2	*
72		Common Control Register 3	CCR3	*
73		Common Control Register 4	CCR4	*
74		Transmit Channel Monitor Select	TDS0SEL	*
75		Transmit DS0 Monitor Register	TDS0M	*
76		Receive Channel Monitor Select	RDS0SEL	*
77		Receive DS0 Monitor Register	RDS0M	*
78		Line Interface Control 1	LIC1	*
79		Line Interface Control 2	LIC2	*
7A		Line Interface Control 3	LIC3	*
7B		Line Interface Control 4	LIC4	*
7C		Test Register	TEST	*
7D		Transmit Line Build-Out Control	TLBC	*
7E		Idle Array Address Register	IAAR	*
7F		Per-Channel Idle Code Value Register	PCICR	*
80		Transmit Idle Code Enable Register 1	TCICE1	*
81		Transmit Idle Code Enable Register 2	TCICE2	*
82		Transmit Idle Code Enable Register 3	TCICE3	*
83		Transmit Idle Code Enable Register 4	TCICE4	*
84		Receive Idle Code Enable Register 1	RCICE1	*
85		Receive Idle Code Enable Register 2	RCICE2	*
86		Receive Idle Code Enable Register 3	RCICE3	*
87		Receive Idle Code Enable Register 4	RCICE4	*
88		Receive Channel Blocking Register 1	RCBR1	*
89		Receive Channel Blocking Register 2	RCBR2	*
8A		Receive Channel Blocking Register 3	RCBR3	*
8B		Receive Channel Blocking Register 4	RCBR4	*
8C		Transmit Channel Blocking Register 1	TCBR1	*
8D		Transmit Channel Blocking Register 2	TCBR2	*

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION	PAGE
8E		Transmit Channel Blocking Register 3	TCBR3	*
8F		Transmit Channel Blocking Register 4	TCBR4	*
90		HDLC #1 Transmit Control	H1TC	*
91		HDLC #1 FIFO Control	H1FC	*
92		HDLC #1 Receive Channel Select 1	H1RCS1	*
93		HDLC #1 Receive Channel Select 2	H1RCS2	*
94		HDLC #1 Receive Channel Select 3	H1RCS3	*
95		HDLC #1 Receive Channel Select 4	H1RCS4	*
96		HDLC #1 Receive Time Slot Bits/Sa Bits Select	H1RTSBS	*
97		HDLC #1 Transmit Channel Select1	H1TCS1	*
98		HDLC #1 Transmit Channel Select 2	H1TCS2	*
99		HDLC #1 Transmit Channel Select 3	H1TCS3	*
9A		HDLC #1 Transmit Channel Select 4	H1TCS4	*
9B		HDLC #1 Transmit Time Slot Bits/Sa Bits Select	H1TTSBS	*
9C		HDLC #1 Receive Packet Bytes Available	H1RPBA	*
9D		HDLC #1 Transmit FIFO	H1TF	*
9E		HDLC #1 Receive FIFO	H1RF	*
9F		HDLC #1 Transmit FIFO Buffer Available	H1TFBA	*
A0		HDLC #2 Transmit Control	H2TC	*
A1		HDLC #2 FIFO Control	H2FC	*
A2		HDLC #2 Receive Channel Select 1	H2RCS1	*
A3		HDLC #2 Receive Channel Select 2	H2RCS2	*
A4		HDLC #2 Receive Channel Select 3	H2RCS3	*
A5		HDLC #2 Receive Channel Select 4	H2RCS4	*
A6		HDLC #2 Receive Time Slot Bits/Sa Bits Select	H2RTSBS	*
A7		HDLC #2 Transmit Channel Select 1	H2TCS1	*
A8		HDLC #2 Transmit Channel Select 2	H2TCS2	*
A9		HDLC #2 Transmit Channel Select 3	H2TCS3	*
AA		HDLC #2 Transmit Channel Select 4	H2TCS4	*
AB		HDLC #2 Transmit Time Slot Bits/Sa Bits Select	H2TTSBS	*
AC		HDLC #2 Receive Packet Bytes Available	H2RPBA	*
AD		HDLC #2 Transmit FIFO	H2TF	*
AE		HDLC #2 Receive FIFO	H2RF	*
AF		HDLC #2 Transmit FIFO Buffer Available	H2TFBA	*
B0		Extend System Information Bus Control Register 1	ESIBCR1	*
B1		Extend System Information Bus Control Register 2	ESIBCR2	*
B2		Extend System Information Bus Register 1	ESIB1	*
B3		Extend System Information Bus Register 2	ESIB2	*
B4		Extend System Information Bus Register 3	ESIB3	*
B5		Extend System Information Bus Register 4	ESIB4	*
B6		In-Band Code Control Register	IBCC	*
B7		Transmit Code Definition Register 1	TCD1	*
B8		Transmit Code Definition Register 2	TCD2	*
B9		Receive Up Code Definition Register 1	RUPCD1	*
BA		Receive Up Code Definition Register 2	RUPCD2	*
BB		Receive Down Code Definition Register 1	RDNCD1	*
BC		Receive Down Code Definition Register 2	RDNCD2	*
BD		In-Band Receive Spare Control Register	RSCC	*
BE		Receive Spare Code Definition Register 1	RSCD1	*
BF		Receive Spare Code Definition Register 2	RSCD2	*
C0		Receive FDL Register	RFDL	*
C1		Transmit FDL Register	TFDL	*

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION	PAGE
C2		Receive FDL Match Register 1	RFDLM1	*
C3		Receive FDL Match Register 2	RFDLM2	*
C4		Test Register	TEST	*
C5		Interleave Bus Operation Control Register	IBOC	*
C6		Receive Align Frame Register	RAF	*
C7		Receive Nonalign Frame Register	RNAF	*
C8		Receive Si Align Frame	RSiAF	*
C9		Receive Si Nonalign Frame	RSiNAF	*
CA		Receive Remote Alarm Bits	RRA	*
CB		Receive Sa4 Bits	RSa4	*
CC		Receive Sa5 Bits	RSa5	*
CD		Receive Sa6 Bits	RSa6	*
CE		Receive Sa7 Bits	RSa7	*
CF		Receive Sa8 Bits	RSa8	*
D0		Transmit Align Frame Register	TAF	*
D1		Transmit Nonalign Frame Register	TNAF	*
D2		Transmit Si Align Frame	TSiAF	*
D3		Transmit Si Nonalign Frame	TSiNAF	*
D4		Transmit Remote Alarm Bits	TRA	*
D5		Transmit Sa4 Bits	TSa4	*
D6		Transmit Sa5 Bits	TSa5	*
D7		Transmit Sa6 Bits	TSa6	*
D8		Transmit Sa7 Bits	TSa7	*
D9		Transmit Sa8 Bits	TSa8	*
DA		Transmit Sa Bit Control Register	TSACR	*
DB		BERT Alternating Word Count Rate	BAWC	*
DC		BERT Repetitive Pattern Set Register 1	BRP1	*
DD		BERT Repetitive Pattern Set Register 2	BRP2	*
DE		BERT Repetitive Pattern Set Register 3	BRP3	*
DF		BERT Repetitive Pattern Set Register 4	BRP4	*
E0		BERT Control Register 1	BC1	*
E1		BERT Control Register 2	BC2	*
E2		Test Register	TEST	*
E3		BERT Bit Count Register 1	BBC1	*
E4		BERT Bit Count Register 2	BBC2	*
E5		BERT Bit Count Register 3	BBC3	*
E6		BERT Bit Count Register 4	BBC4	*
E7		BERT Error Count Register 1	BEC1	*
E8		BERT Error Count Register 2	BEC2	*
E9		BERT Error Count Register 3	BEC3	*
EA		BERT Interface Control Register	BIC	*
EB		Error Rate Control Register	ERC	*
EC		Number Of Errors 1	NOE1	*
ED		Number Of Errors 2	NOE2	*
EE		Number Of Errors Left 1	NOEL1	*
EF		Number Of Errors Left 2	NOEL2	*
F0		Test Register	TEST	*
F1		Test Register	TEST	*
F2		Test Register	TEST	*
F3		Test Register	TEST	*
F4		Test Register	TEST	*
F5		Test Register	TEST	*

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION	PAGE
F6		Test Register	TEST	*
F7		Test Register	TEST	*
F8		Test Register	TEST	*
F9		Test Register	TEST	*
FA		Test Register	TEST	*
FB		Test Register	TEST	*
FC		Test Register	TEST	*
FD		Test Register	TEST	*
FE		Test Register	TEST	*
FF		Test Register	TEST	*

*****TEST1 to TEST16 registers are used only by the factory.

5. SPECIAL PER-CHANNEL REGISTER OPERATION

Some of the features described in the data sheet that operate on a per-channel basis use a special method for channel selection. The registers involved are the per-channel pointer registers (PCPR) and per-channel data registers 1 to 4 (PCDR1–4). The user selects the function(s) that are to be applied on a per-channel basis by setting the appropriate bit(s) in the PCPR register. The user then writes to the PCDR registers to select the channels for that function. The following is an example of mapping the transmit and receive BERT function to channels 9, 10, 11, 12, 20, and 21:

Write 11h to PCPR
Write 00h to PCDR1
Write 0fh to PCDR2
Write 18h to PCDR3
Write 00h to PCDR4

More information about how to use these per-channel features can be found in their respective sections in the data sheet.

Register Name: **PCPR**
Register Description: **Per-Channel Pointer Register**
Register Address: **28h**

Bit #	7	6	5	4	3	2	1	0
Name	RSAOICS	RSRCS	RFCS	BRCS	THSCS	PEICS	TFCS	BTCS
Default	0	0	0	0	0	0	0	0

Bit 0/BERT Transmit Channel Select (BTCS).

Bit 1/Transmit Fractional Channel Select (TFCS).

Bit 2/Payload Error Insert Channel Select (PEICS).

Bit 3/Transmit Hardware Signaling Channel Select (THSCS).

Bit 4/BERT Receive Channel Select (BRCS).

Bit 5/Receive Fractional Channel Select (RFCS).

Bit 6/Receive Signaling Reinsertion Channel Select (RSRCS).

Bit 7/Receive Signaling All Ones Insertion Channel Select (RSAOICS).

Register Name: **PCDR1**
Register Description: **Per-Channel Data Register 1**
Register Address: **29h**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Register Name: **PCDR2**
Register Description: **Per-Channel Data Register 2**
Register Address: **2Ah**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

Register Name: **PCDR3**
Register Description: **Per-Channel Data Register 3**
Register Address: **2Bh**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

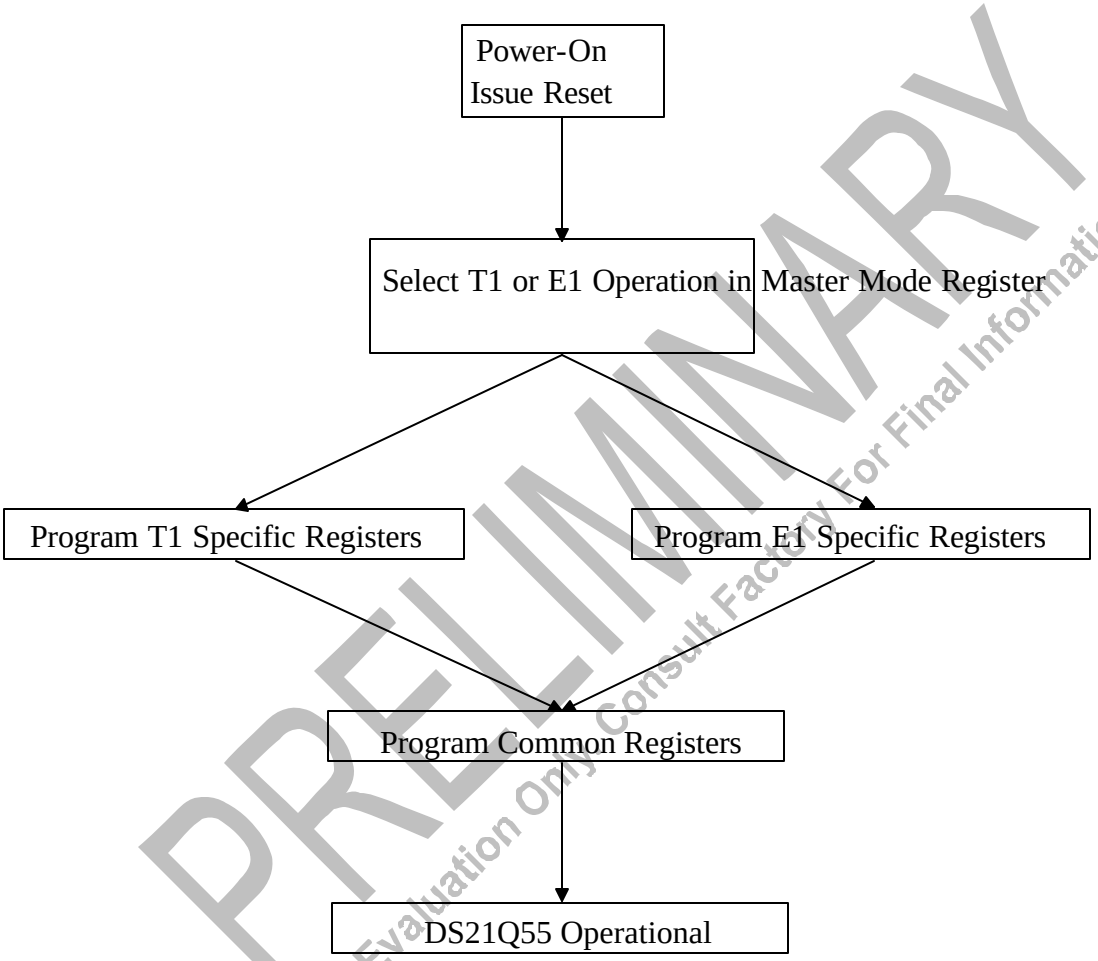
Register Name: **PCDR4**
Register Description: **Per-Channel Data Register 4**
Register Address: **2Ch**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25

6. PROGRAMMING MODEL

The DS21Q55 register map is divided into three groups: T1 specific features, E1 specific features, and common features. The typical programming sequence begins with issuing a reset to the device, selecting T1 or E1 operation in the master mode register, enabling T1 or E1 functions, and enabling the common functions. The act of resetting the device automatically clears all configuration and status registers. Therefore, it is not necessary to load unused registers with zeros.

PROGRAMMING SEQUENCE Figure 8-1



6.1 Power-Up Sequence

The DS21Q55 contains an on-chip power-up reset function, which automatically clears the writeable register space immediately after power is supplied to the device. The user can issue a chip reset at any time. Issuing a reset will disrupt traffic until the device is reprogrammed. The reset can be issued through hardware using the TSTRST pin or through software using the SFTRST function in the master mode register. The LIRST (LIC2.6) should be toggled from zero to one to reset the line interface circuitry. (It will take the DS21Q55 about 40ms to recover from the LIRST bit being toggled.) Finally, after the TSYSCLK and RSYSCLK inputs are stable, the receive and transmit elastic stores should be reset (this step can be skipped if the elastic stores are disabled).

6.1.1 Master Mode Register

Register Name: **MSTRREG**
Register Description: **Master Mode Register**
Register Address: **00h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	TEST1	TEST0	T1/E1	SFTRST
Default	0	0	0	0	0	0	0	0

Bit 0/Software Issued Reset (SFTRST).
A 0 to 1 transition causes the register space to be cleared. A reset clears all configuration and status registers. The bit automatically clears itself when the reset has completed.

Bit 1/Operating Mode (T1/E1).
Used to select the operating mode of the framer/formatter (digital) portion of the 21Q55. The operating mode of the LIU must also be programmed.

0 = T1 operation
1 = E1 operation

Bits 2, 3/Test Mode Bits (TEST0, TEST1).
Test modes are used to force the output pins of the 21Q55 into known states. This can facilitate the checkout of assemblies during the manufacturing process and also be used to isolate devices from shared buses.

TEST1	TEST0	EFFECT ON OUTPUT PINS
0	0	Operate normally
0	1	Force all output pins into tristate (including all I/O pins and parallel port pins)
1	0	Force all output pins low (including all I/O pins except parallel port pins)
1	1	Force all output pins high (including all I/O pins except parallel port pins)

Bits 4–7/Unused, must be set to zero for proper operation.

6.2 Interrupt Handling

Various alarms, conditions, and events in the DS21Q55 can cause interrupts. For simplicity, these are all referred to as events in this explanation. All STATUS registers can be programmed to produce interrupts. Each status register has an associated interrupt mask register. For example, SR1 (Status Register 1) has an interrupt control register called IMR1 (Interrupt Mask Register 1). Status registers are the only sources of interrupts. On power-up, all writeable registers are automatically cleared. Since bits in the IMRx registers have to be set = 1 to allow a particular event to cause an interrupt, no interrupts can occur until the host selects which events are to product interrupts. Since there are potentially many sources of interrupts, several features are available to help sort out and identify which event is causing an interrupt. When an interrupt occurs, the host should first read the IIR1, IIR2, and IIR3 registers (interrupt information registers) to identify which status register(s) is producing the interrupt. Once that is determined, the individual status register or registers can be examined to determine the exact source. In eight port configurations, two DS21Q55s can be connected together via the 3-wire ESIB feature. This allows all eight transceivers to be interrogated by a single CPU port read cycle. The host can determine the synchronization status or interrupt status of all eight devices with a single read. The ESIB feature also allows the user to select from various events to be examined via this method. For more information, see the *ESIB* section in this data sheet.

Once an interrupt has occurred, the interrupt handler routine should set the INTDIS bit (CCR3.6) to stop further activity on the interrupt pin. After all interrupts have been determined and processed, the interrupt hander routine should re-enable interrupts by setting the INTDIS bit = 0.

6.3 Status Registers

When a particular event or condition has occurred (or is still occurring in the case of conditions), the appropriate bit in a status register will be set to a one. All of the status registers operate in a latched fashion, which means that if an event or condition occurs a bit is set to a one. It will remain set until the user reads that bit. An event bit will be cleared when it is read and it will not be set again until the event has occurred again. Condition bits such as RBL, RLOS, etc., will remain set if the alarm is still present.

The user will always proceed a read of any of the status registers with a write. The byte written to the register will inform the DS21Q55 which bits the user wishes to read and have cleared. The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with the latest information. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status registers will be immediately followed by a read of the same register. This write-read scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21Q55 with higher order languages.

Status register bits are divided into two groups, condition bits and event bits. Condition bits are typically network conditions such as loss of sync, or all ones detect. Event bits are typically markers such as the one-second timer, elastic store slip, etc. Each status register bit is labeled as a condition or event bit. Some of the status registers have bits for both the detection of a condition and the clearance of the condition. For example, SR2 has a bit that is set when the device goes into a loss of sync state (SR2.0, a condition bit) and a bit that is set (SR2.4, an event bit) when the loss of sync condition clears (goes in sync). Some of the status register bits (condition bits) do not have a separate bit for the "condition clear" event but rather the status bit can produce interrupts on both edges, setting, and clearing. These bits are

marked as “double interrupt bits.” An interrupt will be produced when the condition occurs and when it clears.

6.4 Information Registers

Information registers operate the same as status registers except they cannot cause interrupts. They are all latched except for INFO7 and some of the bits in INFO5 and INFO6. INFO7 register is a read only register and it reports the status of the E1 synchronizer in real time. INFO7 and some of the bits in INFO6 and INFO5 are not latched and it is not necessary to precede a read of these bits with a write.

6.5 Interrupt Information Registers

The Interrupt Information Registers provide an indication of which Status Registers (SR1 through SR9) are generating an interrupt. When an interrupt occurs, the host can read IIR1 and IIR2 to quickly identify which of the 9 status registers are causing the interrupt.

Register Name: **IIR1**
Register Description: **Interrupt Information Register 1**
Register Address: **14h**

Bit #	7	6	5	4	3	2	1	0
Name	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1
Default	0	0	0	0	0	0	0	0

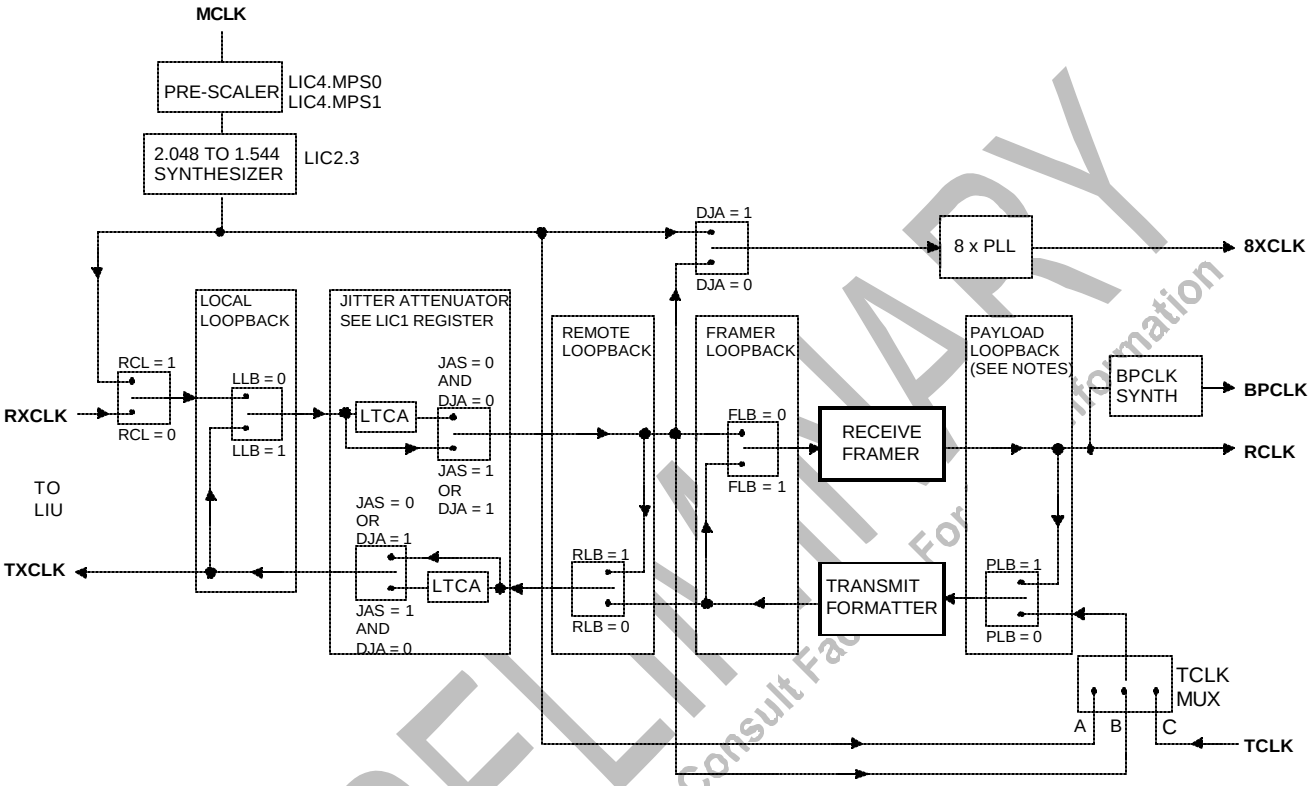
Register Name: **IIR2**
Register Description: **Interrupt Information Register 2**
Register Address: **15h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	SR9
Default	0	0	0	0	0	0	0	0

7. CLOCK MAP

Figure 9-1 shows the clock map of the DS21Q55. The routing for the transmit and receive clocks are shown for the various loopback modes and jitter attenuator positions. Although there is only one jitter attenuator, which can be placed in the receive or transmit path, two are shown for simplification and clarity.

CLOCK MAP Figure 9-1



The TCLK MUX is dependent on the state of the TCSS0 and TCSS1 bits in the LIC1 register and the state of the TCLK pin.

TCSS1	TCSS0	TRANSMIT CLOCK SOURCE
0	0	The TCLK pin (C) is always the source of Transmit Clock.
0	1	Switch to the recovered clock (B) when the signal at the TCLK pin fails to transition after 1 channel time.
1	0	Use the scaled signal (A) derived from MCLK as the Transmit Clock. The TCLK pin is ignored.
1	1	Use the recovered clock (B) as the Transmit Clock. The TCLK pin is ignored.

8. T1 FRAMER/FORMATTER CONTROL REGISTERS

The T1 framer portion of the DS21Q55 is configured via a set of nine control registers. Typically, the control registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two receive-control registers (T1RCR1 and T1RCR2), two transmit control registers (T1TCR1 and T1TCR2), and a common control register (T1CCR1). Each of these registers is described in this section.

8.1 T1 Control Registers

Register Name: **T1RCR1**
Register Description: **T1 Receive Control Register 1**
Register Address: **03h**

Bit #	7	6	5	4	3	2	1	0
Name	-	ARC	OOF1	OOF2	SYNCC	SYNCT	SYNCE	RESYNC
Default	0	0	0	0	0	0	0	0

Bit 0/Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

Bit 1/Sync Enable (SYNCE).
0 = auto resync enabled
1 = auto resync disabled

Bit 2/Sync Time (SYNCT).
0 = qualify 10 bits
1 = qualify 24 bits

Bit 3/Sync Criteria (SYNCC).
In D4 Framing Mode.
0 = search for Ft pattern, then search for Fs pattern
1 = cross couple Ft and Fs pattern
In ESF Framing Mode.
0 = search for FPS pattern only
1 = search for FPS and verify with CRC6

Bits 4 to 5/Out Of Frame Select Bits (OOF2, OOF1).

OOF2	OOF1	OUT OF FRAME CRITERIA
0	0	2/4 frame bits in error
0	1	2/5 frame bits in error
1	0	2/6 frame bits in error
1	1	2/6 frame bits in error

Bit 6/Auto Resync Criteria (ARC).
0 = resync on OOF or RCL event
1 = resync on OOF only

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **T1RCR2**
Register Description: **T1 Receive Control Register 2**
Register Address: **04h**

Bit #	7	6	5	4	3	2	1	0
Name	-	RFM	RB8ZS	RSLC96	RZSE	RZBTSI	RJC	RD4YM
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Side D4 Yellow Alarm Select (RD4YM).
0 = zeros in bit 2 of all channels
1 = a one in the S-bit position of frame 12 (J1 Yellow Alarm Mode)

Bit 1/Receive Japanese CRC6 Enable (RJC).
0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)
1 = use Japanese standard JT–G704 CRC6 calculation

Bit 2/Receive Side ZBTSI Support Enable (RZBTSI). Allows ZBTSI information to be output on RLINK pin.
0 = ZBTSI disabled
1 = ZBTSI enabled

Bit 3/Receive FDL Zero Destuffer Enable (RZSE). Set this bit to zero if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See *Legacy FDL Support (T1 Mode)* for details.
0 = zero destuffer disabled
1 = zero destuffer enabled

Bit 4/Receive SLC–96 Enable (RSLC96). Only set this bit to a one in SLC–96 framing applications. See *D4/SLC–96 Operation* for details.
0 = SLC–96 disabled
1 = SLC–96 enabled

Bit 5/Receive B8ZS Enable (RB8ZS).
0 = B8ZS disabled
1 = B8ZS enabled

Bit 6/Receive Frame Mode Select (RFM).
0 = D4 framing mode
1 = ESF framing mode

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **T1TCR1**
Register Description: **T1 Transmit Control Register 1**
Register Address: **05h**

Bit #	7	6	5	4	3	2	1	0
Name	TJC	TFPT	TCPT	TSSE	GB7S	TFDLS	TBL	TYEL
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit Yellow Alarm (TYEL).
0 = do not transmit yellow alarm
1 = transmit yellow alarm

Bit 1/Transmit Blue Alarm (TBL).
0 = transmit data normally
1 = transmit an unframed all one's code at TPOS and TNEG

Bit 2/TFDL Register Select (TFDLS).
0 = source FDL or Fs bits from the internal TFDL register (legacy FDL support mode)
1 = source FDL or Fs bits from the internal HDLC controller or the TLINK pin

Bit 3/Global Bit 7 Stuffing (GB7S).
0 = allow the SSIEx registers to determine which channels containing all zeros are to be Bit 7 stuffed
1 = force Bit 7 stuffing in all zero byte channels regardless of how the SSIEx registers are programmed

Bit 4/Transmit Software Signaling Enable (TSSE).
0 = do not source signaling data from the TSx registers regardless of the SSIEx registers. The SSIEx registers still define which channels are to have B7 stuffing preformed
1 = source signaling data as enabled by the SSIEx registers

Bit 5/Transmit CRC Pass Through (TCPT).
0 = source CRC6 bits internally
1 = CRC6 bits sampled at TSER during F-bit time

Bit 6/Transmit F-Bit Pass Through (TFPT).
0 = F bits sourced internally
1 = F bits sampled at TSER

Bit 7/Transmit Japanese CRC6 Enable (TJC).
0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)
1 = use Japanese standard JT–G704 CRC6 calculation

Register Name: **T1TCR2**
Register Description: **T1 Transmit Control Register 2**
Register Address: **06h**

Bit #	7	6	5	4	3	2	1	0
Name	TB8ZS	TSLC96	TZSE	FBCT2	FBCT1	TD4YM	TZBTSI	TB7ZS
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit Side Bit 7 Zero Suppression Enable (TB7ZS).
0 = no stuffing occurs
1 = Bit 7 force to a one in channels with all zeros

Bit 1/Transmit Side ZBTSI Support Enable (TZBTSI). Allows ZBTSI information to be input on TLINK pin.
0 = ZBTSI disabled
1 = ZBTSI enabled

Bit 2/Transmit Side D4 Yellow Alarm Select (TD4YM).
0 = zeros in bit 2 of all channels
1 = a one in the S-bit position of frame 12

Bit 3/F-Bit Corruption Type 1. (FBCT1). A low-to-high transition of this bit causes the next three consecutive Ft (D4 framing mode) or FPS (ESF framing mode) bits to be corrupted, causing the remote end to experience a loss of synchronization.

Bit 4/F-Bit Corruption Type 2. (FBCT2). Setting this bit high enables the corruption of one Ft (D4 framing mode) or FPS (ESF framing mode) bit in every 128 Ft or FPS bits as long as the bit remains set.

Bit 5/Transmit FDL Zero Stuffer Enable (TZSE). Set this bit to zero if using the internal HDLC controller instead of the legacy support for the FDL. See *I/O Pin Configuration Options* for details.
0 = zero stuffer disabled
1 = zero stuffer enabled

Bit 6/Transmit SLC–96/Fs-Bit Insertion Enable (TSLC96). Only set this bit to a one in D4 framing and SLC-96 applications. Must be set to one to source the Fs pattern from the TFDL register. See *D4/SLC–96 Operation* for details.
0 = SLC–96/Fs-bit insertion disabled
1 = SLC–96/Fs-bit insertion enabled

Bit 7/Transmit B8ZS Enable (TB8ZS).
0 = B8ZS disabled
1 = B8ZS enabled

Register Name: **T1CCR1**
Register Description: **T1 Common Control Register 1**
Register Address: **07h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	TFM	PDE	TLOOP
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit Loop Code Enable (TLOOP). See *Programmable In-Band Loop Codes Generation and Detection* for details.
0 = transmit data normally
1 = replace normal transmitted data with repeating code as defined in registers TCD1 and TCD2

Bit 1/Pulse Density Enforcer Enable (PDE). The framer always examines both the transmit and receive data streams for violations of the following rules, which are required by ANSI T1.403: no more than 15 consecutive zeros and at least N ones in each and every time window of 8 x (N +1) bits where N = 1 through 23. Violations for the transmit and receive data streams are reported in the INFO1.6 and INFO1.7 bits respectively. When this bit is set to one, the device will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, this bit should be set to zero since B8ZS encoded data streams cannot violate the pulse density requirements.
0 = disable transmit pulse density enforcer
1 = enable transmit pulse density enforcer

Bit 2/Transmit Frame Mode Select (TFM).
0 = D4 framing mode
1 = ESF framing mode

Bit 3/Unused, must be set to zero for proper operation.

Bit 4/Unused, must be set to zero for proper operation.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

8.2 T1 Transmit Transparency

The software-signaling insertion-enable registers, SSIE1–SSIE4, can be used to select signaling insertion from the transmit-signaling registers, TS1–TS12, on a per-channel basis. Setting a bit in the SSIEx register allows signaling data to be sourced from the signaling registers for that channel.

In transparent mode, bit 7 stuffing and/or robbed-bit signaling is prevented from overwriting the data in the channels. If a DS0 is programmed to be clear, no robbed-bit signaling will be inserted nor will the channel have bit 7 stuffing performed. However, in the D4 framing mode, bit 2 will be overwritten by a zero when a yellow alarm is transmitted. Also, the user has the option to globally override the SSIEx registers from determining which channels are to have bit 7 stuffing performed. If the T1TCR1.3 and T1TCR2.0 bits are set to one, then all 24 T1 channels will have bit 7 stuffing performed on them, regardless of how the SSIEx registers are programmed. In this manner, the SSIEx registers are only affecting channels that are to have robbed-bit signaling inserted into them.

8.3 T1 Receive-Side Digital-Milliwatt Code Generation

Receive-side digital-milliwatt code generation involves using the receive digital-milliwatt registers (T1RDMR1/2/3) to determine which of the 24 T1 channels of the T1 line going to the backplane should be overwritten with a digital-milliwatt pattern. The digital-milliwatt code is an 8-byte repeating pattern that represents a 1kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). Each bit in the T1RDMRx registers represents a particular channel. If a bit is set to a one, then the receive data in that channel will be replaced with the digital-milliwatt code. If a bit is set to zero, no replacement occurs.

Register Name: **T1RDMR1**
Register Description: **T1 Receive Digital Milliwatt Enable Register 1**
Register Address: **0Ch**

Bit #	7	6	5	4	3	2	1	0
Name	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Digital Milliwatt Enable for Channels 1 to 8 (CH1 to CH8).
0 = do not affect the receive data associated with this channel
1 = replace the receive data associated with this channel with digital-milliwatt code

Register Name: **T1RDMR2**
Register Description: **T1 Receive Digital Milliwatt Enable Register 2**
Register Address: **0Dh**

Bit #	7	6	5	4	3	2	1	0
Name	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Digital Milliwatt Enable for Channels 9 to 16 (CH9 to CH16).
0 = do not affect the receive data associated with this channel
1 = replace the receive data associated with this channel with digital-milliwatt code

Register Name: **T1RDMR3**
Register Description: **T1 Receive Digital Milliwatt Enable Register 3**
Register Address: **0Eh**

Bit #	7	6	5	4	3	2	1	0
Name	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Digital Milliwatt Enable for Channels 17 to 24 (CH17 to CH24).
0 = do not affect the receive data associated with this channel
1 = replace the receive data associated with this channel with digital-milliwatt code

8.4 T1 Information Register

Register Name: **INFO1**
Register Description: **Information Register 1**
Register Address: **10h**

Bit #	7	6	5	4	3	2	1	0
Name	RPDV	TPDV	COFA	8ZD	16ZD	SEFE	B8ZS	FBE
Default	0	0	0	0	0	0	0	0

Bit 0/Frame Bit Error Event (FBE). Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

Bit 1/B8ZS Code Word Detect Event (B8ZS). Set when a B8ZS code word is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via T1TCR2.7. Useful for automatically setting the line coding.

Bit 2/Severely Errored Framing Event (SEFE). Set when two out of six framing bits (Ft or FPS) are received in error.

Bit 3/Sixteen Zero Detect Event (16ZD). Set when a string of at least 16 consecutive zeros (regardless of the length of the string) have been received at RPOSI and RNEGI.

Bit 4/Eight Zero Detect Event (8ZD). Set when a string of at least eight consecutive zeros (regardless of the length of the string) have been received at RPOSI and RNEGI.

Bit 5/Change of Frame Alignment Event (COFA). Set when the last resync resulted in a change of frame or multiframe alignment.

Bit 6/Transmit Pulse Density Violation Event (TPDV). Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

Bit 7/Receive Pulse Density Violation Event (RPDV). Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.

T1 ALARM CRITERIA Table 10-1

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (Note 1)	Over a 3ms window, five or fewer zeros are received	Over a 3ms window, six or more zeros are received
Yellow Alarm (RAI)		
D4 Bit-2 Mode (T1RCR2.0 = 0)	Bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences	Bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences
D4 12th F-bit Mode (T1RCR2.0 = 1; this mode is also referred to as the "Japanese Yellow Alarm")	12th framing bit is set to one for two consecutive occurrences	12th framing bit is set to zero for two consecutive occurrences
ESF Mode	16 consecutive patterns of 00FF appear in the FDL	14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL
Red Alarm (LRCL) (Also referred to as Loss Of Signal)	192 consecutive zeros are received	14 or more ones out of 112 possible bit positions are received, starting with the first one received

NOTES:

1) The definition of blue alarm (or alarm indication signal) is an unframed, all-ones signal. Blue alarm detectors should be able to operate properly in the presence of a 10E-3 error rate, and they should not falsely trigger on a framed, all-ones signal. The blue alarm criteria in the DS21Q55 has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS bit.
2) ANSI specifications use a different nomenclature than this data sheet does; the following terms are equivalent:

RBL = AIS
RCL = LOS
RLOS = LOF
RYEL = RAI

9. E1 FRAMER/FORMATTER CONTROL REGISTERS

The E1 framer portion of the DS21Q55 is configured via a set of four control registers. Typically, the control registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two receive control registers (E1RCR1 and E1RCR2) and two transmit control registers (E1TCR1 and E1TCR2). There are also four status and information registers. Each of these eight registers are described in this section.

9.1 E1 Control Registers

Register Name: **E1RCR1**
Register Description: **E1 Receive Control Register 1**
Register Address: **33h**

Bit #	7	6	5	4	3	2	1	0
Name	RSERC	RSIGM	RHDB3	RG802	RCRC4	FRC	SYNCE	RESYNC
Default	0	0	0	0	0	0	0	0

Bit 0/Resync (RESYNC). When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

Bit 1/Sync Enable (SYNCE).
0 = auto resync enabled
1 = auto resync disabled

Bit 2/Frame Resync Criteria (FRC).
0 = resync if FAS received in error 3 consecutive times
1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times

Bit 3/Receive CRC4 Enable (RCRC4).
0 = CRC4 disabled
1 = CRC4 enabled

Bit 4/Receive G.802 Enable (RG802). See *Signaling Operation* for details.
0 = do not force RCHBLK high during bit 1 of timeslot 26
1 = force RCHBLK high during bit 1 of timeslot 26

Bit 5/Receive HDB3 Enable (RHDB3).
0 = HDB3 disabled
1 = HDB3 enabled

Bit 6/Receive Signaling Mode Select (RSIGM).
0 = CAS signaling mode
1 = CCS signaling mode

Bit 7/RSER Control (RSERC).
0 = allow RSER to output data as received under all conditions
1 = force RSER to one under loss of frame alignment conditions

E1 SYNC/RESYNC CRITERIA Table 11-1

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N + 2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate: (E1RCR1.2 = 1) The above criteria is met or three consecutive incorrect bit 2 of non-FAS received	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found and previous timeslot 16 contains code other than all zeros	Two consecutive MF alignment words received in error	G.732 5.2

Register Name: **E1RCR2**
Register Description: **E1 Receive Control Register 2**
Register Address: **34h**

Bit #	7	6	5	4	3	2	1	0
Name	Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	-	-	RCLA
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Carrier Loss (RCL) Alternate Criteria (RCLA). Defines the criteria for a Receive Carrier Loss condition for both the framer and Line Interface (LIU)
0 = RCL declared upon 255 consecutive zeros (125µs)
1 = RCL declared upon 2048 consecutive zeros (1ms)

Bit 1/Unused, must be set to zero for proper operation.

Bit 2/Unused, must be set to zero for proper operation.

Bit 3/Sa4-Bit Select(Sa4S). Set to one to have RLCLK pulse at the Sa4-bit position; set to zero to force RLCLK low during Sa4-bit position. See *Functional Timing Diagrams* for details.

Bit 4/Sa5-Bit Select(Sa5S). Set to one to have RLCLK pulse at the Sa5-bit position; set to zero to force RLCLK low during Sa5-bit position. See *Functional Timing Diagrams* for details.

Bit 5/Sa6-Bit Select(Sa6S). Set to one to have RLCLK pulse at the Sa6-bit position; set to zero to force RLCLK low during Sa6-bit position. See *Functional Timing Diagrams* for details.

Bit 6/Sa7-Bit Select(Sa7S). Set to one to have RLCLK pulse at the Sa7-bit position; set to zero to force RLCLK low during Sa7-bit position. See *Functional Timing Diagrams* for details.

Bit 7/Sa8-Bit Select (Sa8S). Set to one to have RLCLK pulse at the Sa8-bit position; set to zero to force RLCLK low during Sa8-bit position. See *Functional Timing Diagrams* for details.

Register Name: **E1TCR1**
Register Description: **E1 Transmit Control Register 1**
Register Address: **35h**

Bit #	7	6	5	4	3	2	1	0
Name	TFPT	T16S	TUA1	TSiS	TSA1	THDB3	TG802	TCRC4
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit CRC4 Enable (TCRC4).
0 = CRC4 disabled
1 = CRC4 enabled

Bit 1/Transmit G.802 Enable (TG802). See *Functional Timing Diagrams* for details.
0 = do not force TCHBLK high during bit 1 of timeslot 26
1 = force TCHBLK high during bit 1 of timeslot 26

Bit 2/Transmit HDB3 Enable (THDB3).
0 = HDB3 disabled
1 = HDB3 enabled

Bit 3/Transmit Signaling All Ones (TSA1).
0 = normal operation
1 = force timeslot 16 in every frame to all ones

Bit 4/Transmit International Bit Select (TSiS).
0 = sample Si bits at TSER pin
1 = source Si bits from TAF and TNAF registers (in this mode, E1TCR1.7 must be set to zero)

Bit 5/Transmit Unframed All Ones (TUA1).
0 = transmit data normally
1 = transmit an unframed all one's code at TPOSO and TNEGO

Bit 6/Transmit Timeslot 16 Data Select (T16S). See *Transmit Signaling* for details
0 = timeslot 16 determined by the SSIEx registers and the THSCS function in the PCPR register
1 = source timeslot 16 from TS1 to TS16 registers

Bit 7/Transmit Timeslot 0 Pass Through (TFPT).
0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers
1 = FAS bits/Sa bits/Remote Alarm sourced from TSER

Register Name: **E1TCR2**
Register Description: **E1 Transmit Control Register 2**
Register Address: **36h**

Bit #	7	6	5	4	3	2	1	0
Name	Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	AEBE	AAIS	ARA
Default	0	0	0	0	0	0	0	0

Bit 0/Automatic Remote Alarm Generation (ARA).
0 = disabled
1 = enabled

Bit 1/Automatic AIS Generation (AAIS).
0 = disabled
1 = enabled

Bit 2/Automatic E-Bit Enable (AEBE).
0 = E-bits not automatically set in the transmit direction
1 = E-bits automatically set in the transmit direction

Bit 3/Sa4-Bit Select (Sa4S). Set to one to source the Sa4 bit from the TLINK pin; set to zero to not source the Sa4 bit. See *Functional Timing Diagrams* for details.

Bit 4/Sa5-Bit Select (Sa5S). Set to one to source the Sa5 bit from the TLINK pin; set to zero to not source the Sa5 bit. See *Functional Timing Diagrams* for details.

Bit 5/Sa6-Bit Select (Sa6S). Set to one to source the Sa6 bit from the TLINK pin; set to zero to not source the Sa6 bit. See *Functional Timing Diagrams* for details.

Bit 6/Sa7-Bit Select (Sa7S). Set to one to source the Sa7 bit from the TLINK pin; set to zero to not source the Sa7 bit. See *Functional Timing Diagrams* for details.

Bit 7/Sa8-Bit Select (Sa8S). Set to one to source the Sa8 bit from the TLINK pin; set to zero to not source the Sa8 bit. See *Functional Timing Diagrams* for details.

9.2 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or remote alarm. When automatic AIS generation is enabled (E1TCR2.1 = 1), the device monitors the receive side framer to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all ones) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the framer will either force an AIS or remote alarm.

When automatic RAI generation is enabled (E1TCR2.0 = 1), the framer monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all ones) reception, or loss of receive carrier (or signal) or if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled). If any one (or more) of the above conditions is present, then the framer will transmit a RAI alarm. RAI generation conforms to ETS 300 011 specifications and a constant remote alarm will be transmitted if the DS21Q55 cannot find CRC4 multiframe synchronization within 400ms as per G.706.

Note: It is an illegal state to have both automatic AIS generation and automatic remote alarm generation enabled at the same time.

9.3 E1 Information Registers

Register Name: **INFO3**
Register Description: **Information Register 3**
Register Address: **12h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	CRCRC	FASRC	CASRC
Default	0	0	0	0	0	0	0	0

Bit 0/CAS Resync Criteria Met Event (CASRC). Set when two consecutive CAS MF alignment words are received in error.

Bit 1/FAS Resync Criteria Me t Event (FASRC. Set when three consecutive FAS words are received in error.

Bit 2/CRC Resync Criteria Met Event (CRCRC). Set when 915/1000 code words are received in error.

Register Name: **INFO7**
Register Description: **Information Register 7 (Real Time)**
Register Address: **30h**

Bit #	7	6	5	4	3	2	1	0
Name	CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA
Default	0	0	0	0	0	0	0	0

Bit 0/CRC4 MF Sync Active (CRC4SA). Set while the synchronizer is searching for the CRC4 MF alignment word.

Bit 1/CAS MF Sync Active (CASSA). Set while the synchronizer is searching for the CAS MF alignment word.

Bit 2/FAS Sync Active (FASSA). Set while the synchronizer is searching for alignment at the FAS level.

Bit 3 to 7/CRC4 Sync Counter Bits (CSC0 and CSC2 to CSC4). The CRC4 sync counter increments each time the 8ms-CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (E1RCR1.3 = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400ms, then the search should be abandoned and proper action taken. The CRC4 sync counter will rollover. CSC0 is the LSB of the 6-bit counter. (**Note:** The second LSB, CSC1, is not accessible. CSC1 is omitted to allow resolution to >400ms using 5 bits.)

E1 ALARM CRITERIA Table 11-2

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RLOS	An **RLOS** condition exists on power-up prior to initial synchronization, when a re-sync criteria has been met, or when a manual re-sync has been initiated via E1RCR1.0		
RCL	255 or 2048 consecutive zeros received as determined by E1RCR2.0	In 255-bit times, at least 32 ones are received	G.775/G.962
RRA	Bit 3 of nonalign frame set to one for three consecutive occasions	Bit 3 of nonalign frame set to zero for three consecutive occasions	O.162 2.1.4
RUA1	Fewer than three zeros in two frames (512 bits)	More than two zeros in two frames (512 bits)	O.162 1.6.1.2
RDMA	Bit 6 of timeslot 16 in frame 0 has been set for two consecutive multiframes		
V52LNK	Two out of three Sa7 bits are zero		G.965

10. COMMON CONTROL AND STATUS REGISTERS

Register Name: **CCR1**
Register Description: **Common Control Register 1**
Register Address: **70h**

Bit #	7	6	5	4	3	2	1	0
Name	-	CRC4R	SIE	ODM	DICAI	TCSS1	TCSS0	RLOSF
Default	0	0	0	0	0	0	0	0

Bit 0/Function of the RLOS/LOTC Output (RLOSF).
0 = Receive Loss of Sync (RLOS)
1 = Loss of Transmit Clock (LOTC)

Bit 1/Transmit Clock Source Select bit 0 (TCSS0).

Bit 2/Transmit Clock Source Select bit 1 (TCSS1).

TCSS1	TCSS0	TRANSMIT CLOCK SOURCE
0	0	The TCLK pin is always the source of transmit clock.
0	1	Switch to the clock present at RCLK when the signal at the TCLK pin fails to transition after one channel time.
1	0	Use the scaled signal present at MCLK as the transmit clock. The TCLK pin is ignored.
1	1	Use the signal present at RCLK as the transmit clock. The TCLK pin is ignored.

Bit 3/Disable Idle Code Auto Increment (DICAI) Selects/deselects the auto increment feature for the transmit and receive idle code array address register.
0 = addresses in IAAR register automatically increment on every read/write operation to the PCICR register
1 = addresses in IAAR register do not automatically increment

Bit 4/Output Data Mode (ODM).
0 = pulses at TPOSO and TNEGO are one full TCLKO period wide
1 = pulses at TPOSO and TNEGO are 1/2 TCLKO period wide

Bit 5/Signaling Integration Enable (SIE).
0 = signaling changes of state reported on any change in selected channels
1 = signaling must be stable for three multiframes in order for a change of state to be reported

Bit 6/CRC-4 Recalcul ate (CRC4R). (E1 Only)
0 = transmit CRC-4 generation and insertion operates in normal mode
1 = transmit CRC-4 generation operates according to G.706 Intermediate Path Recalculation method

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **IDR**
Register Description: **Device Identification Register**
Register Address: **0Fh**

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default	1	0	1	1	X	X	X	X

Bits 0 to 3/Chip Revision Bits (ID0 to ID3). The lower four bits of the IDR are used to display the die revision of the chip. IDO is the LSB of a decimal code that represents the chip revision.

Bits 4 to 7/Device ID (ID4 to ID7). The upper four bits of the IDR are used to display the device ID.

Register Name: **SR2**
Register Description: **Status Register 2**
Register Address: **18h**

Bit #	7	6	5	4	3	2	1	0
Name	RYELC	RUA1C	FRCLC	RLOSC	RYEL	RUA1	FRCL	RLOS
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Loss of Sync Condition (RLOS). Set when the device is not synchronized to the received data stream.

Bit 1/Framer Receive Carrier Loss Condition (FRCL). Set when 255 (or 2048 if E1RCR2.0 = 1) E1 mode or 192 T1 mode consecutive zeros have been detected at RPOSI and RNEGI.

Bit 2/Receive Unframed All Ones (T1, Blue Alarm, E1, AIS) Condition (RUA1). Set when an unframed all ones code is received at RPOSI and RNEGI.

Bit 3/Receive Yellow Alarm Condition (RYEL). (T1 only) Set when a yellow alarm is received at RPOSI and RNEGI.

Bit 4/Receive Loss of Sync Clear Event (RLOSC). Set when the framer achieves synchronization; will remain set until read.

Bit 5/Framer Receive Carrier Loss Clear Event (FRCLC). Set when carrier loss condition at RPOSI and RNEGI is no longer detected.

Bit 6/Receive Unframed All Ones Clear Event (RUA1C). Set when the unframed all ones condition is no longer detected.

Bit 7/Receive Yellow Alarm Clear Event (RYELC). (T1 only) Set when the yellow alarm condition is no longer detected.

Register Name: **IMR2**
Register Description: **Interrupt Mask Register 2**
Register Address: **19h**

Bit #	7	6	5	4	3	2	1	0
Name	RYELC	RUA1C	FRCLC	RLOSC	RYEL	RUA1	FRCL	RLOS
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Loss of Sync Condition (RLOS).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 1/Framer Receive Carrier Loss Condition (FRCL).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 2/Receive Unframed All Ones (Blue Alarm) Condition (RUA1).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 3/Receive Yellow Alarm Condition (RYEL).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 4/Receive Loss of Sync Clear Event (RLOSC).
0 = interrupt masked
1 = interrupt enabled

Bit 5/Framer Receive Carrier Loss Condition Clear (FRCLC).
0 = interrupt masked
1 = interrupt enabled

Bit 6/Receive Unframed All Ones Condition Clear Event (RUA1C).
0 = interrupt masked
1 = interrupt enabled

Bit 7/Receive Yellow Alarm Clear Event (RYELC).
0 = interrupt masked
1 = interrupt enabled

Register Name: **SR3**
Register Description: **Status Register 3**
Register Address: **1Ah**

Bit #	7	6	5	4	3	2	1	0
Name	LSPARE	LDN	LUP	LOTC	LORC	V52LNK	RDMA	RRA
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Remote Alarm Condition (RRA). (E1 only) Set when a remote alarm is received at RPOSI and RNEGI

Bit 1/Receive Distant MF Alarm Condition (RDMA). (E1 only) Set when bit 6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.

Bit 2/V5.2 Link Detected Condition (V52LNK). (E1 only) Set on detection of a V5.2 link identification signal. (G.965).

Bit 3/Loss of Receive Clock Condition (LORC). Set when the RCLKI pin has not transitioned for one channel time.

Bit 4/Loss of Transmit Clock Condition (LOTC). Set when the TCLK pin has not transitioned for one channel time. Will force the LOTC pin high if enabled via CCR1.0.

Bit 5/Loop Up Code Detected Condition (LUP). (**T1 only)** Set when the loop up code as defined in the RUPCD1/2 register is being received. See *Programmable In-Band Loop Code Generation and Detection* for details.

Bit 6/Loop Down Code Detected Condition (LDN). (T1 only) Set when the loop down code as defined in the RDNCD1/2 register is being received. See *Programmable In-Band Loop Code Generation and Detection* for details.

Bit 7/Spare Code Detected Condition (LSPARE). (T1 only) Set when the spare code as defined in the RSCD1/2 registers is being received. See *Programmable In-Band Loop Code Generation and Detection* for details.

Register Name: **IMR3**
Register Description: **Interrupt Mask Register 3**
Register Address: **1Bh**

Bit #	7	6	5	4	3	2	1	0
Name	LSPARE	LDN	LUP	LOTC	LORC	V52LNK	RDMA	RRA
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Remote Alarm Condition (RRA).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 1/Receive Distant MF Alarm Condition (RDMA).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 2/V5.2 Link Detected Condition (V52LNK).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 3/Loss of Receive Clock Condition (LORC).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 4/Loss of Transmit Clock Condition (LOTC).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 5/Loop Up Code Detected Condition (LUP).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 6/Loop Down Code Detected Condition (LDN).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 7/Spare Code Detected Condition (LSPARE).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Register Name: **SR4**
Register Description: **Status Register 4**
Register Address: **1Ch**

Bit #	7	6	5	4	3	2	1	0
Name	-	RSA1	RSA0	TMF	TAF	RMF	RCMF	RAF
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Align Frame Event (RAF). (E1 only) Set every 250µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.

Bit 1/Receive CRC4 Multiframe Event (RCMF). (E1 only) Set on CRC4 multiframe boundaries; will continue to be set every 2ms on an arbitrary boundary if CRC4 is disabled.

Bit 2/Receive Multiframe Event (RMF).
E1 Mode: Set every 2ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 3/Transmit Align Frame Event (TAF). (E1 only) Set every 250µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.

Bit 4/Transmit Multiframe Event (TMF).
E1 Mode: Set every 2ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 5/Receive Signaling All Zeros Event (RSA0). (E1 only) Set when over a full MF, timeslot 16 contains all zeros.

Bit 6/Receive Signaling All Ones Event (RSA1). (E1 only) Set when the contents of timeslot 16 contains fewer than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.

Register Name: **IMR4**
Register Description: **Interrupt Mask Register 4**
Register Address: **1Dh**

Bit #	7	6	5	4	3	2	1	0
Name	-	RSA1	RSA0	TMF	TAF	RMF	RCMF	RAF
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Align Frame Event (RAF).
0 = interrupt masked
1 = interrupt enabled

Bit 1/Receive CRC4 Multiframe Event (RCMF).
0 = interrupt masked
1 = interrupt enabled

Bit 2/Receive Multiframe Event (RMF).
0 = interrupt masked
1 = interrupt enabled

Bit 3/Transmit Align Frame Event (TAF).
0 = interrupt masked
1 = interrupt enabled

Bit 4/Transmit Multiframe Event (TMF).
0 = interrupt masked
1 = interrupt enabled

Bit 5/Receive Signaling All Zeros Event (RSA0).
0 = interrupt masked
1 = interrupt enabled

Bit 6/Receive Signaling All Ones Event (RSA1).
0 = interrupt masked
1 = interrupt enabled

11. I/O PIN CONFIGURATION OPTIONS

Register Name: **IOCR1**
Register Description: **I/O Configuration Register 1**
Register Address: **01h**

Bit #	7	6	5	4	3	2	1	0
Name	RSMS	RSMS2	RSMS1	RSIO	TSDW	TSM	TSIO	ODF
Default	0	0	0	0	0	0	0	0

Bit 0/Output Data Format (ODF).
0 = bipolar data at TPOSO and TNEGO
1 = NRZ data at TPOSO; TNEGO = 0

Bit 1/TSYNC I/O Select (TSIO).
0 = TSYNC is an input
1 = TSYNC is an output

Bit 2/TSYNC Mode Select (TSM). Selects frame or multiframe mode for the TSYNC pin.
0 = frame mode
1 = multiframe mode

Bit 3/TSYNC Double-Wide (TSDW). (T1 only) (Note: this bit must be set to zero when IOCR1.2 = 1 or when IOCR1.1 = 0)
0 = do not pulse double-wide in signaling frames
1 = do pulse double-wide in signaling frames

Bit 4/RSYNC I/O Select (RSIO). (Note: this bit must be set to zero when ESCR.0 = 0)
0 = RSYNC is an output
1 = RSYNC is an input (only valid if elastic store enabled)

Bit 5/RSYNC Mode Select 1(RSMS1). Selects frame or multiframe pulse when RSYNC pin is in output mode. In input mode (elastic store must be enabled) multiframe mode is only useful when receive signaling re-insertion is enabled.
0 = frame mode
1 = multiframe mode

Bit 6/RSYNC Mode Select 2(RSMS2).
T1 Mode: RSYNC pin must be programmed in the output frame mode (IOCR1.5 = 0, IOCR1.4 = 0).
0 = do not pulse double wide in signaling frames
1 = do pulse double wide in signaling frames
E1 Mode: RSYNC pin must be programmed in the output multiframe mode
(IOCR1.5 = 1, IOCR1.4 = 0).
0 = RSYNC outputs CAS multiframe boundaries
1 = RSYNC outputs CRC4 multiframe boundaries

Bit 7/RSYNC Multiframe Skip Control (RSMS). Useful in framing format conversions from D4 to ESF. This function is not available when the receive-side elastic store is enabled. RSYNC must be set to output multiframe pulses (IOCR1.5 = 1 and IOCR1.4 = 0).
0 = RSYNC will output a pulse at every multiframe
1 = RSYNC will output a pulse at every other multiframe

Register Name: **IOCR2**
Register Description: **I/O Configuration Register 2**
Register Address: **02h**

Bit #	7	6	5	4	3	2	1	0
Name	RCLKINV	TCLKINV	RSYNCINV	TSYNCINV	TSSYNCINV	H100EN	TSCLKM	RSCLKM
Default	0	0	0	0	0	0	0	0

Bit 0/RSYSCLK Mode Select (RSCLKM).
0 = if RSYSCLK is 1.544MHz
1 = if RSYSCLK is 2.048MHz or IBO enabled (See *Interleaved PCM Bus Operation.*)

Bit 1/TSYSCLK Mode Select (TSCLKM).
0 = if TSYSCLK is 1.544MHz
1 = if TSYSCLK is 2.048MHz or IBO enabled (See *Interleaved PCM Bus Operation.*)

Bit 2/H.100 SYNC Mode (H100EN).
0 = normal operation
1 = SYNC shift

Bit 3/TSSYNC Invert (TSSYNCINV).
0 = no inversion
1 = invert

Bit 4/TSYNC Invert (TSYNCINV).
0 = no inversion
1 = invert

Bit 5/RSYNC Invert (RSYNCINV).
0 = no inversion
1 = invert

Bit 6/TCLK Invert (TCLKINV).
0 = no inversion
1 = invert

Bit 7/RCLK Invert (RCLKINV).
0 = no inversion
1 = invert

12. LOOPBACK CONFIGURATION

Register Name: **LBCR**
Register Description: **Loopback Control Register**
Register Address: **4Ah**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	LIUC	LLB	RLB	PLB	FLB
Default	0	0	0	0	0	0	0	0

Bit 0/Framer Loopback (FLB).
0 = loopback disabled
1 = loopback enabled

This loopback is useful in testing and debugging applications. In FLB, the device will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1) T1 Mode: An unframed all ones code will be transmitted at TPOSO and TNEGO.
   E1 Mode: Normal data will be transmitted at TPOSO and TNEGO.
2) Data at RPOSI and RNEGI will be ignored.
3) All receive side signals will take on timing synchronous with TCLK instead of RCLKI.
4) Please note that it is not acceptable to have RCLK tied to TCLK during this loopback because this will cause an unstable condition.

Bit 1/Payload Loopback (PLB).
0 = loopback disabled
1 = loopback enabled

When PLB is enabled, the following will occur:

1) Data will be transmitted from the TPOSO and TNEGO pins synchronous with RCLK instead of TCLK.
2) All of the receive side signals will continue to operate normally.
3) The TCHCLK and TCHBLK signals are forced low.
4) Data at the TSER and TSIG pins is ignored.
5) The TLCLK signal will become synchronous with RCLK instead of TCLK.

T1 Mode: Normally, this loopback is only enabled when ESF framing is being performed but can be enabled also in D4 framing applications. In a PLB situation, the device will loop the 192 bits of pay-load data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the device.

E1 Mode: In a PLB situation, the device will loop the 248 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The transmit section will modify the payload as if it was input at TSER. The FAS word, Si, Sa and E bits, and CRC4 are not looped back, they are reinserted by the device.

Bit 2/Remote Loopback (RLB). In this loopback, data input via the RPOSI and RNEGI pins will be transmitted back to the TPOSO and TNEGO pins. Data will continue to pass through the receive side framer of the device as it would normally and the data from the transmit side formatter will be ignored.
0 = loopback disabled
1 = loopback enabled

Bit 3/Local Loopback (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the device. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator. (See Figure 1-1 *Line Interface Unit*.)

0 = loopback disabled
1 = loopback enabled

Bit 4/Line Interface Unit Mux Control (LIUC). This is a software version of the LIUC pin. When the LIUC pin is connected high the LIUC bit has control. When the LIUC pin is connected low the framer and LIU are separated and the LIUC bit has no effect.

0 = if LIUC pin connected high, LIU internally connected to framer block and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins.
1 = if LIUC pin connected high, disconnect LIU from framer block and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins.

LIUC pin	LIUC bit	
0	0	LIU and Framer Separated
0	1	LIU and Framer Separated
1	0	LIU and Framer Connected
1	1	LIU and Framer Separated

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

12.1 Per-Channel Loopback

The per-channel loopback registers (PCLRs) determine which channels (if any) from the backplane should be replaced with the data from the receive side or in other words, off of the T1 or E1 line. If this loopback is enabled, then transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this would be to tie RCLK to TCLK and RFSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Each of the bit position in the PCLRs (PCLR1/PCLR2/PCLR3/PCLR4) represent a DS0 channel in the outgoing frame. When these bits are set to a one, data from the corresponding receive channel will replace the data on TSER for that channel.

Register Name: **PCLR1**
Register Description: **Per-Channel Loopback Enable Register 1**
Register Address: **4Bh**

Bit #	7	6	5	4	3	2	1	0
Name	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Per-Channel Loopback Enable for Channels 1 to 8 (CH1 to CH8).
0 = loopback disabled
1 = enable loopback. Source data from the corresponding receive channel

Register Name: **PCLR2**
Register Description: **Per-Channel Loopback Enable Register 2**
Register Address: **4Ch**

Bit #	7	6	5	4	3	2	1	0
Name	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Per-Channel Loopback Enable for Channels 9 to 16 (CH9 to CH16).
0 = loopback disabled
1 = enable loopback. Source data from the corresponding receive channel

Register Name: **PCLR3**
Register Description: **Per-Channel Loopback Enable Register 3**
Register Address: **4Dh**

Bit #	7	6	5	4	3	2	1	0
Name	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Per-Channel Loopback Enable for Channels 17 to 24 (CH17 to CH24).
0 = loopback disabled
1 = enable loopback. Source data from the corresponding receive channel

Register Name: **PCLR4**
Register Description: **Per-Channel Loopback Enable Register 4**
Register Address: **4Eh**

Bit #	7	6	5	4	3	2	1	0
Name	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Per-Channel Loopback Enable for Channels 25 to 32 (CH25 to CH32).
0 = loopback disabled
1 = enable loopback. Source data from the corresponding receive channel

13. ERROR COUNT REGISTERS

The DS21Q55 contains four counters that are used to accumulate line coding errors, path errors, and synchronization errors. Counter update options include one second boundaries, 42ms (T1 mode only), 62ms (E1 mode only) or manually. See Error Counter Configuration Register (ERCNT). When updated automatically, the user can use the interrupt from the timer to determine when to read these registers. All four counters will saturate at their respective maximum counts and they will not rollover (**Note**: Only the line-code violation-count register has the potential to overflow but the bit error would have to exceed 10E-2 before this would occur).

Register Name: **ERCNT**
Register Description: **Error Counter Configuration Register**
Register Address: **41h**

Bit #	7	6	5	4	3	2	1	0
Name	-	MECU	ECUS	EAMS	VCRFS	FSBE	MOSCRF	LCVCRF
Default	0	0	0	0	0	0	0	0

Bit 0/T1 Line Code Violation Count Register Function Select (LCVCRF).
0 = do not count excessive zeros
1 = count excessive zeros

Bit 1/Multiframe Out of Sync Count Register Function Select (MOSCRF).
0 = count errors in the framing bit position
1 = count the number of multiframes out of sync

Bit 2/PCVCR Fs-Bit Error Report Enable (FSBE).
0 = do not report bit errors in Fs-bit position; only Ft-bit position
1 = report bit errors in Fs-bit position as well as Ft-bit position

Bit 3/E1 Line Code Violation Count Register Function Select (VCRFS).
0 = count BiPolar Violations (BPVs)
1 = count Code Violations (CVs)

Bit 4/Error Accumulation Mode Select (EAMS).
0 = ERCNT.5 determines accumulation time
1 = ERCNT.6 determines accumulation time

Bit 5/Error Counter Update Select (ECUS).
T1 Mode**:** 0 = Update error counters once a second
1 = Update error counters every 42ms (333 frames)
E1 Mode: 0 = Update error counters once a second
1 = Update error counters every 62.5ms (500 frames)

Bit 6/Manual Error Counter Update (MECU). When enabled by ERCNT.4, the changing of this bit from a zero to a one allows the next clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of 1.5 RCLK clock periods before reading the error count registers to allow for proper update.

Bit 7/Unused, must be set to zero for proper operation.

13.1 Line Code Violation Count Register (LCVCR)

T1 Operation

T1 code violations are defined as bipolar violations (BPVs) or excessive zeros. If the B8ZS mode is set for the receive side, then B8ZS code words are not counted. This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS = 1) conditions (Table 15-1).

T1 LINE CODE VIOLATION COUNTING OPTIONS Table 15-1

COUNT EXCESSIVE ZEROS? (ERCNT.0)	B8ZS ENABLED? (T1RCR2.5)	WHAT IS COUNTED IN THE LCVCRs
No	No	BPVs
Yes	No	BPVs + 16 Consecutive Zeros
No	Yes	BPVs (B8ZS Code Words Not Counted)
Yes	Yes	BPVs + 8 Consecutive Zeros

E1 Operation

Either bipolar violations or code violations can be counted. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side, then HDB3 code words are not counted as BPVs. If ERCNT.3 is set, then the LVC counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on an E1 line would have to be greater than 10** -2 before the VCR would saturate (Table 15-2).

E1 LINE CODE VIOLATION COUNTING OPTIONS Table 15-2

E1 CODE VIOLATION SELECT (ERCNT.3)	WHAT IS COUNTED IN THE LCVCRs
0	BPVs
1	CVs

Register Name: **LCVCR1**
Register Description: **Line Code Violation Count Register 1**
Register Address: **42h**

Bit #	7	6	5	4	3	2	1	0
Name	LCVC15	LCVC14	LCVC13	LCVC12	LCVC11	LCVC10	LCVC9	LCCV8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Line Code Violation Counter Bits 8 to 15 (LCVC8 to LCVC15). LCV15 is the MSB of the 16-bit code violation count.

Register Name: **LCVCR2**
Register Description: **Line Code Violation Count Register 2**
Register Address: **43h**

Bit #	7	6	5	4	3	2	1	0
Name	LCVC7	LCVC6	LCVC5	LCVC4	LCVC3	LCVC2	LCVC1	LCVC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Line Code Violation Counter Bits 0 to 7 (LCVC0 to LCVC7). LCV0 is the LSB of the 16-bit code violation count.

13.2 Path Code Violation Count Register (PCVCR)

T1 Operation

The path-code violation-count register records either Ft, Fs, or CRC6 errors in T1 frames. When the receive side of a framer is set to operate in the T1 ESF framing mode, PCVCR will record errors in the CRC6 code words. When set to operate in the T1 D4 framing mode, PCVCR will count errors in the Ft framing bit position. Via the ERCNT.2 bit, a framer can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS = 1) conditions. See Table 15-3 for a detailed description of exactly what errors the PCVCR counts.

T1 PATH CODE VIOLATION COUNTING ARRANGEMENTS Table 15-3

FRAMING MODE	COUNT Fs ERRORS?	WHAT IS COUNTED IN THE PCVCRs
D4	No	Errors in the Ft Pattern
D4	Yes	Errors in Both the Ft and Fs Patterns
ESF	Don't Care	Errors in the CRC6 Code Words

E1 Operation

The PCVCR records CRC4 errors. Since the maximum CRC4 count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

The PCVCR1 is the most significant word and PCVCR2 is the least significant word of a 16-bit counter that records path violations (PVs).

Register Name: **PCVCR1**
Register Description: **Path Code Violation Count Register 1**
Register Address: **44h**

Bit #	7	6	5	4	3	2	1	0
Name	PCVC15	PCVC14	PCVC13	PCVC12	PCVC11	PCVC10	PCVC9	PCVC8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Path Code Violation Counter Bits 8 to 15 (PCVC8 to PCVC15). PCVC15 is the MSB of the 16-bit path code violation count.

Register Name: **PCVCR2**
Register Description: **Path Code Violation Count Register 2**
Register Address: **45h**

Bit #	7	6	5	4	3	2	1	0
Name	PCVC7	PCVC6	PCVC5	PCVC4	PCVC3	PCVC2	PCVC1	PCVC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Path Code Violation Counter Bits 0 to 7 (PCVC0 to PCVC7). PCVC0 is the LSB of the 16-bit path code violation count.

13.3 Frames Out Of Sync Count Register (FOSCR)

T1 Operation

The FOSCR is used to count the number of multiframes that the receive synchronizer is out of sync. This number is useful in ESF applications needing to measure the parameters loss of frame count (LOFC) and ESF error events as described in AT&T publication TR54016. When the FOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOS = 1) conditions. The FOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the FOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS = 1) conditions. See Table 15-4 for a detailed description of what the FOSCR is capable of counting.

T1 FRAMES OUT OF SYNC COUNTING ARRANGEMENTS Table 15-4

FRAMING MODE (T1RCR1.3)	COUNT MOS OR F-BIT ERRORS (ERCNT.1)	WHAT IS COUNTED IN THE FOSCRs
D4	MOS	Number of Multiframes Out of Sync
D4	F-Bit	Errors in the Ft Pattern
ESF	MOS	Number of Multiframes Out of Sync
ESF	F-Bit	Errors in the FPS Pattern

E1 Operation

The FOSCR counts word errors in the frame alignment signal in timeslot 0. This counter is disabled when RLOS is high. FAS errors will not be counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one-second period is 4000, this counter cannot saturate.

The FOSCR1 (FOSCR1) is the most significant word and FOSCR2 is the least significant word of a 16-bit counter that records frames out of sync.

Register Name: **FOSCR1**
Register Description: **Frames Out Of Sync Count Register 1**
Register Address: **46h**

Bit #	7	6	5	4	3	2	1	0
Name	FOS15	FOS14	FOS13	FOS12	FOS11	FOS10	FOS9	FOS8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Frames Out of Sync Counter Bits 8 to 15 (FOS8 to FOS15). FOS15 is the MSB of the 16-bit frames out of sync count.

Register Name: **FOSCR2**
Register Description: **Frames Out Of Sync Count Register 2**
Register Address: **47h**

Bit #	7	6	5	4	3	2	1	0
Name	FOS7	FOS6	FOS5	FOS4	FOS3	FOS2	FOS1	FOS0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Frames Out of Sync Counter Bits 0 to 7 (FOS0 to FOS7). FOS0 is the LSB of the 16-bit frames out of sync count.

13.4 E-Bit Counter Register (EBCR)

This counter is only available in the E1 mode. EBCR1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 16-bit counter that records far end block errors (FEBE), as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E-bit is set to zero. Since the maximum E-bit count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

Register Name: **EBCR1**
Register Description: **E-Bit Count Register 1**
Register Address: **48h**

Bit #	7	6	5	4	3	2	1	0
Name	EB15	EB14	EB13	EB12	EB11	EB10	EB9	EB8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/E-Bit Counter Bits 8 to 15 (EB8 to EB15). EB15 is the MSB of the 16-bit E-bit count.

Register Name: **EBCR2**
Register Description: **E-Bit Count Register 2**
Register Address: **49h**

Bit #	7	6	5	4	3	2	1	0
Name	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/E-Bit Counter Bits 0 to 7 (EB0 to EB7). EB0 is the LSB of the 16-bit E-bit count.

14. DS0 MONITORING FUNCTION

The DS21Q55 has the ability to monitor one DS0 64kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the TDS0SEL register. In the receive direction, the RCM0 to RCM4 bits in the RDS0SEL register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the transmit DS0 monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate T1 or E1 channel. T1 channels 1 through 24 map to register values 0 through 23. E1 channels 1 through 32 map to register values 0 through 31. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into TDS0SEL and RDS0SEL:

TCM4 = 0	RCM4 = 0
TCM3 = 0	RCM3 = 1
TCM2 = 1	RCM2 = 1
TCM1 = 0	RCM1 = 1
TCM0 = 1	RCM0 = 0

14.1 Transmit DS0 Monitor Registers

Register Name: **TDS0SEL**
Register Description: **Transmit Channel Monitor Select**
Register Address: **74h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	TCM4	TCM3	TCM2	TCM1	TCM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 Transmit Channel Monitor Bits (TCM0 to TCM4). TCM0 is the LSB of a 5-bit channel select that determines which transmit channel data will appear in the TDS0M register.

Bits 5 to 7/Unused, must be set to zero for proper operation.

Register Name: **TDS0M**
Register Description: **Transmit DS0 Monitor Register**
Register Address: **75h**

Bit #	7	6	5	4	3	2	1	0
Name	B1	B2	B3	B4	B5	B6	B7	B8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit DS0 Channel Bits (B1 to B8). Transmit channel data that has been selected by the transmit channel monitor select register. B8 is the LSB of the DS0 channel (last bit to be transmitted).

14.2 Receive DS0 Monitor Registers

Register Name: **RDS0SEL**
Register Description: **Receive Channel Monitor Select**
Register Address: **76h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	RCM4	RCM3	RCM2	RCM1	RCM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4/Receive Channel Monitor Bits (RCM0 to RCM4). RCM0 is the LSB of a 5-bit channel-select that determines which receive DS0 channel data will appear in the RDS0M register.

Bits 5 to 7/Unused, must be set to zero for proper operation.

Register Name: **RDS0M**
Register Description: **Receive DS0 Monitor Register**
Register Address: **77h**

Bit #	7	6	5	4	3	2	1	0
Name	B1	B2	B3	B4	B5	B6	B7	B8
Default	0	0	0	0	0	0	0	0

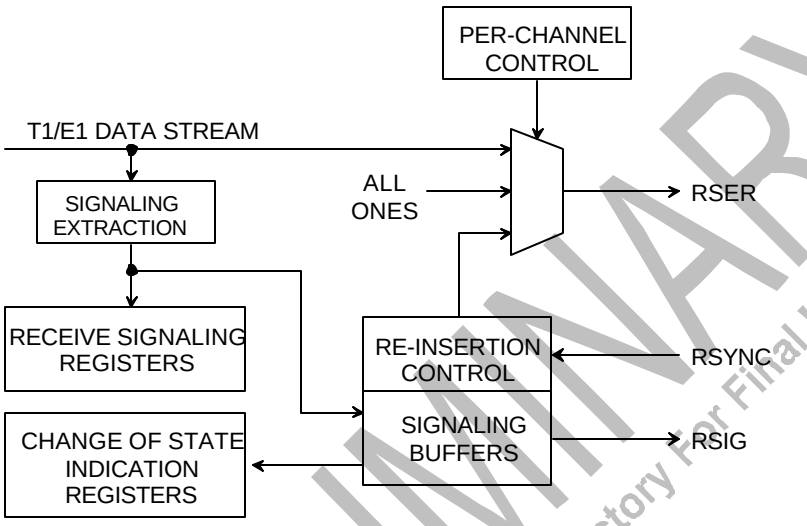
Bits 0 to 7/Receive DS0 Channel Bits (B1 to B8). Receive-channel data that has been selected by the receive-channel monitor-select register. B8 is the LSB of the DS0 channel (last bit to be received).

15. SIGNALING OPERATION

There are two methods to access receive signaling data and provide transmit signaling data: processor-based (i.e., software-based) or hardware-based. Processor-based refers to access through the transmit and receive signaling registers, RS1–RS16 and TS1–TS16. Hardware-based refers to the TSIG and RSIG pins. Both methods can be used simultaneously.

15.1 Receive Signaling

SIMPLIFIED DIAGRAM OF RECEIVE SIGNALING PATH Figure 17-1



15.1.1 Processor-Based Receive Signaling

The robbed-bit signaling (T1) or TS16 CAS signaling (E1) is sampled in the receive data stream and copied into the receive signaling registers, RS1 through RS16. In T1 mode, only RS1 through RS12 are used. The signaling information in these registers is always updated on multiframe boundaries. This function is always enabled.

15.1.1.1 Change Of State

In order to avoid constant monitoring of the receive signaling registers, the DS21Q55 can be programmed to alert the host when any specific channel or channels undergo a change of their signaling state. RSCSE1 through RSCSE4 for E1 and RSCSE1 through RSCSE3 for T1 are used to select which channels can cause a change of state indication. The change of state is indicated in Status Register 5 (SR1.5). If signaling integration, CCR1.5, is enabled then the new signaling state must be constant for three multiframes before a change of state indication is indicated. The user can enable the INT pin to toggle low upon detection of a change in signaling by setting the IMR1.5 bit. The signaling integration mode is global and cannot be enabled on a channel by channel basis.

The user can identity which channels have undergone a signaling change of state by reading the RSINFO1 through RSINFO4 registers . The information from this registers will tell the user which RSx register to read for the new signaling data. All changes are indicated in the RSINFO1–RSINFO4 register regardless of the RSCSE1–RSCSE4 registers.

15.1.2 Hardware-Based Receive Signaling

In hardware-based signaling the signaling data can be obtained from the RSER pin or the RSIG pin. RSIG is a signaling PCM-stream output on a channel-by-channel basis from the signaling buffer. The signaling data, T1 robbed bit or E1 TS16, is still present in the original data stream at RSER. The signaling buffer provides signaling data to the RSIG pin and also allows signaling data to be reinserted into the original data stream in a different alignment that is determined by a multiframe signal from the RSYNC pin. In this mode, the receive elastic store can be enabled or disabled. If the receive elastic store is enabled, then the backplane clock (RSYSCLK) can be either 1.544MHz or 2.048MHz. In the ESF framing mode, the ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once a multiframe (3ms) unless a freeze is in effect. In the D4 framing mode, the AB signaling bits are output twice on RSIG in the lower nibble of each channel. Hence, bits 5 and 6 contain the same data as bits 7 and 8 respectively in each channel. The RSIG data is updated once a multiframe (1.5ms) unless a freeze is in effect. See the *Functional Timing Diagrams* for some examples.

15.1.2.1 Receive-Signaling Reinsertion at RSER

In this mode, the user will provide a multiframe sync at the RSYNC pin and the signaling data will be reinserted based on this alignment. In T1 mode, this results in two copies of the signaling data in the RSER data stream. The original signaling data based on the Fs/ESF frame positions and the realigned data based on the user supplied multiframe sync applied at RSYNC. In voice channels this extra copy of signaling data is of little consequence. Reinsertion can be avoided in data channels since this feature is activated on a per-channel basis. For reinsertion, the elastic store must be enabled; however, the backplane clock can be either 1.544MHz or 2.048MHz.

Signaling reinsertion mode is enabled, on a per-channel basis by setting the RSRCS bit high in the PCPR register. The channels that are to have signaling reinserted are selected by writing to the PCDR1-PCDR3

registers for T1 mode and PCDR1-PCDR4 registers for E1 mode. In E1 mode, the user will generally select all channels when doing reinsertion.

15.1.2.2 Force Receive Signaling All Ones

In T1 mode, the user can, on a per-channel basis, force the robbed-bit signaling-bit positions to a one. This is done by using the per-channel register, which is described in the *Special Per-Channel Operation* section. The user sets the BTCS bit in the PCPR register. The channels that are to be forced to one are selected by writing to the PCDR1-PCDR3 registers.

15.1.2.3 Receive-Signaling Freeze

The signaling data in the four-multiframe signaling buffer will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or frame slip. This action meets the requirements of BellCore TR–TSY–000170 for signaling freezing. To allow this freeze action to occur, the RFE control bit (SIGCR.4) should be set high. The user can force a freeze by setting the RFF control bit (SIGCR.3) high. The RSIGF output pin provides a hardware indication that a freeze is in effect. The four multiframe buffer provides a three-multiframe delay in the signaling bits provided at the RSIG pin (and at the RSER pin if receive signaling reinsertion is enabled). When freezing is enabled (RFE = 1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data will be held in the old state for at least an additional 9ms (or 4.5ms in D4 framing mode) before being allowed to be updated with new signaling data.

Register Name: **SIGCR**
Register Description: **Signaling Control Register**
Register Address: **40h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	RFE	RFF	-	-	-
Default	0	0	0	0	0	0	0	0

Bit 0/Unused, must be set to zero for proper operation.

Bit 1/Unused, must be set to zero for proper operation.

Bit 2/Unused, must be set to zero for proper operation.

Bit 3/Receive Force Freeze (RFF). Freezes receive-side signaling at RSIG (and RSER if receive signaling reinsertion is enabled); will override receive-freeze enable (RFE). See *Receive Signaling Freeze.*

0 = do not force a freeze event
1 = force a freeze event

Bit 4/Receive Freeze Enable (RFE). See *Receive Signaling Freeze.*

0 = no freezing of receive signaling data will occur
1 = allow freezing of receive signaling data at RSIG (and RSER if receive signaling reinsertion is enabled).

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **RS1 to RS12**
Register Description: **Receive Signaling Registers (T1 Mode, ESF Format)**
Register Address: **60h to 6Bh**

(MSB)							(LSB)	
CH2-A	CH2-B	CH2-C	CH2-D	CH1-A	CH1-B	CH1-C	CH1-D	RS1
CH4-A	CH4-B	CH4-C	CH4-D	CH3-A	CH3-B	CH3-C	CH3-D	RS2
CH6-A	CH6-B	CH6-C	CH6-D	CH5-A	CH5-B	CH5-C	CH5-D	RS3
CH8-A	CH8-B	CH8-C	CH8-D	CH7-A	CH7-B	CH7-C	CH7-D	RS4
CH10-A	CH10-B	CH10-C	CH10-D	CH9-A	CH9-B	CH9-C	CH9-D	RS5
CH12-A	CH12-B	CH12-C	CH12-D	CH11-A	CH11-B	CH11-C	CH11-D	RS6
CH14-A	CH14-B	CH14-C	CH14-D	CH13-A	CH13-B	CH13-C	CH13-D	RS7
CH16-A	CH16-B	CH16-C	CH16-D	CH15-A	CH15-B	CH15-C	CH15-D	RS8
CH18-A	CH18-B	CH18-C	CH18-D	CH17-A	CH17-B	CH17-C	CH17-D	RS9
CH20-A	CH20-B	CH20-C	CH20-D	CH19-A	CH19-B	CH19-C	CH19-D	RS10
CH22-A	CH22-B	CH22-C	CH22-D	CH21-A	CH21-B	CH21-C	CH21-D	RS11
CH24-A	CH24-B	CH24-C	CH24-D	CH23-A	CH23-B	CH23-C	CH23-D	RS12

Register Name: **RS1 to RS12**
Register Description: **Receive Signaling Registers (T1 Mode, D4 Format)**
Register Address: **60h to 6Bh**

(MSB)							(LSB)	
CH2-A	CH2-B	**CH2-A**	**CH2-B**	CH1-A	CH1-B	**CH1-A**	**CH1-B**	RS1
CH4-A	CH4-B	**CH4-A**	**CH4-B**	CH3-A	CH3-B	**CH3-A**	**CH3-B**	RS2
CH6-A	CH6-B	**CH6-A**	**CH6-B**	CH5-A	CH5-B	**CH5-A**	**CH5-B**	RS3
CH8-A	CH8-B	**CH8-A**	**CH8-B**	CH7-A	CH7-B	**CH7-A**	**CH7-B**	RS4
CH10-A	CH10-B	**CH10-A**	**CH10-B**	CH9-A	CH9-B	**CH9-A**	**CH9-B**	RS5
CH12-A	CH12-B	**CH12-A**	**CH12-B**	CH11-A	CH11-B	**CH11-A**	**CH11-B**	RS6
CH14-A	CH14-B	**CH14-A**	**CH14-B**	CH13-A	CH13-B	**CH13-A**	**CH13-B**	RS7
CH16-A	CH16-B	**CH16-A**	**CH16-B**	CH15-A	CH15-B	**CH15-A**	**CH15-B**	RS8
CH18-A	CH18-B	**CH18-A**	**CH18-B**	CH17-A	CH17-B	**CH17-A**	**CH17-B**	RS9
CH20-A	CH20-B	**CH20-A**	**CH20-B**	CH19-A	CH19-B	**CH19-A**	**CH19-B**	RS10
CH22-A	CH22-B	**CH22-A**	**CH22-B**	CH21-A	CH21-B	**CH21-A**	**CH21-B**	RS11
CH24-A	CH24-B	**CH24-A**	**CH24-B**	CH23-A	CH23-B	**CH23-A**	**CH23-B**	RS12

Note: In D4 format, TS1-TS12 contain signaling data for two frames. Bold type indicates data for second frame.

Register Name: **RS1 to RS16**
Register Description: **Receive Signaling Registers (E1 Mode, CAS Format)**
Register Address: **60h to 6Fh**

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	RS1
CH2-A	CH2-B	CH2-C	CH2-D	CH1-A	CH1-B	CH1-C	CH1-D	RS2
CH4-A	CH4-B	CH4-C	CH4-D	CH3-A	CH3-B	CH3-C	CH3-D	RS3
CH6-A	CH6-B	CH6-C	CH6-D	CH5-A	CH5-B	CH5-C	CH5-D	RS4
CH8-A	CH8-B	CH8-C	CH8-D	CH7-A	CH7-B	CH7-C	CH7-D	RS5
CH10-A	CH10-B	CH10-C	CH10-D	CH9-A	CH9-B	CH9-C	CH9-D	RS6
CH12-A	CH12-B	CH12-C	CH12-D	CH11-A	CH11-B	CH11-C	CH11-D	RS7
CH14-A	CH14-B	CH14-C	CH14-D	CH13-A	CH13-B	CH13-C	CH13-D	RS8
CH16-A	CH16-B	CH16-C	CH16-D	CH15-A	CH15-B	CH15-C	CH15-D	RS9
CH18-A	CH18-B	CH18-C	CH18-D	CH17-A	CH17-B	CH17-C	CH17-D	RS10
CH20-A	CH20-B	CH20-C	CH20-D	CH19-A	CH19-B	CH19-C	CH19-D	RS11
CH22-A	CH22-B	CH22-C	CH22-D	CH21-A	CH21-B	CH21-C	CH21-D	RS12
CH24-A	CH24-B	CH24-C	CH24-D	CH23-A	CH23-B	CH23-C	CH23-D	RS13
CH26-A	CH26-B	CH26-C	CH26-D	CH25-A	CH25-B	CH25-C	CH25-D	RS14
CH28-A	CH28-B	CH28-C	CH28-D	CH27-A	CH27-B	CH27-C	CH27-D	RS15
CH30-A	CH30-B	CH30-C	CH30-D	CH29-A	CH29-B	CH29-C	CH29-D	RS16

Register Name: **RSCSE1, RSCSE2, RSCSE3, RSCSE4**
Register Description: **Receive Signaling Change Of State Interrupt Enable**
Register Address: **3Ch, 3Dh, 3Eh, 3Fh**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RSCSE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSCSE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RSCSE3**
		CH30	CH29	CH28	CH27	CH26	CH25	**RSCSE4**

Setting any of the CH1 through CH30 bits in the RSCSE1 through RSCSE4 registers will cause an interrupt when that channel's signaling data changes state.

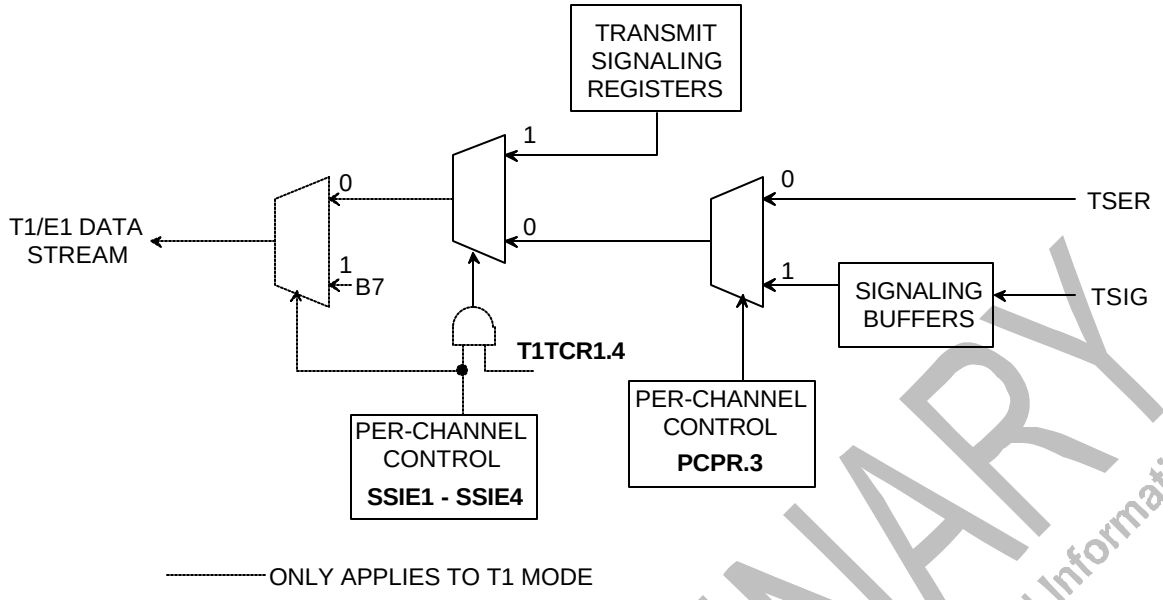
Register Name: **RSINFO1, RSINFO2, RSINFO3, RSINFO4**
Register Description: **Receive Signaling Change Of State Information**
Register Address: **38h, 39h, 3Ah, 3Bh**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RSINFO1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSINFO2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RSINFO3**
		CH30	CH29	CH28	CH27	CH26	CH25	**RSINFO4**

When a channel's signaling data changes state, the respective bit in registers RSINFO1-4 will be set. If the channel was also enabled as an interrupt source by setting the appropriate bit in RSCSE1–4, an interrupt is generated. The bit will remain set until read.

15.2 Transmit Signaling

SIMPLIFIED DIAGRAM OF TRANSMIT SIGNALING PATH Figure 17-2



15.2.1 Processor-Based Transmit Signaling

In processor-based mode, signaling data is loaded into the transmit-signaling registers (TS1–TS16) via the host interface. On multiframe boundaries, the contents of these registers is loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can utilize the transmit multiframe interrupt in status register 4 (SR4.4) to know when to update the signaling bits. The user need not update any transmit signaling register for which there is no change of state for that register.

Each transmit signaling register contains the robbed-bit signaling (T1) or TS16 CAS signaling (E1) for two timeslots that will be inserted into the outgoing stream if enabled to do so via T1TCR1.4 (T1 Mode) or E1TCR1.6 (E1 Mode). In T1 mode, only TS1 through TS12 are used.

Signaling data can be sourced from the TS registers on a per-channel basis by utilizing the software-signaling insertion-enable registers, SSIE1 through SSIE4.

15.2.1.1 T1 Mode

In T1 ESF framing mode, there are four signaling bits per channel (A, B, C, and D). TS1–TS12 contain a full multiframe of signaling data. In T1 D4 framing mode, there are only two signaling bits per channel (A and B). In T1 D4 framing mode, the framer uses the C and D bit positions as the A and B bit positions for the next multiframe. In D4 mode, two multiframes of signaling data can be loaded into TS1–TS12.

The framer will load the contents of TS1–TS12 into the outgoing shift register every other D4 multiframe. In D4 mode the host should load new contents into TS1–TS12 on every other multiframe boundary and no later than 120µs after the boundary.

15.2.1.2 E1 Mode

In E1 mode, TS16 carries the signaling information. This information can be in either CCS (common channel signaling) or CAS (channel associated signaling) format. The 32 time slots are referenced by two different channel number schemes in E1. In channel numbering, TS0 through TS31 are labeled channels 1 through 32. In phone-channel numbering, TS1 through TS15 are labeled channel 1 through channel 15, and TS17 through TS31 are labeled channel 15 through channel 30.

TIME SLOT NUMBERING SCHEMES Table 17-1

TS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Phone Channel		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

Register Name: **TS1 to TS16**
Register Description: **Transmit Signaling Registers (E1 Mode, CAS Format)**
Register Address: **50h to 5Fh**

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	TS1
CH2-A	CH2-B	CH2-C	CH2-D	CH1-A	CH1-B	CH1-C	CH1-D	TS2
CH4-A	CH4-B	CH4-C	CH4-D	CH3-A	CH3-B	CH3-C	CH3-D	TS3
CH6-A	CH6-B	CH6-C	CH6-D	CH5-A	CH5-B	CH5-C	CH5-D	TS4
CH8-A	CH8-B	CH8-C	CH8-D	CH7-A	CH7-B	CH7-C	CH7-D	TS5
CH10-A	CH10-B	CH10-C	CH10-D	CH9-A	CH9-B	CH9-C	CH9-D	TS6
CH12-A	CH12-B	CH12-C	CH12-D	CH11-A	CH11-B	CH11-C	CH11-D	TS7
CH14-A	CH14-B	CH14-C	CH14-D	CH13-A	CH13-B	CH13-C	CH13-D	TS8
CH16-A	CH16-B	CH16-C	CH16-D	CH15-A	CH15-B	CH15-C	CH15-D	TS9
CH18-A	CH18-B	CH18-C	CH18-D	CH17-A	CH17-B	CH17-C	CH17-D	TS10
CH20-A	CH20-B	CH20-C	CH20-D	CH19-A	CH19-B	CH19-C	CH19-D	TS11
CH22-A	CH22-B	CH22-C	CH22-D	CH21-A	CH21-B	CH21-C	CH21-D	TS12
CH24-A	CH24-B	CH24-C	CH24-D	CH23-A	CH23-B	CH23-C	CH23-D	TS13
CH26-A	CH26-B	CH26-C	CH26-D	CH25-A	CH25-B	CH25-C	CH25-D	TS14
CH28-A	CH28-B	CH28-C	CH28-D	CH27-A	CH27-B	CH27-C	CH27-D	TS15
CH30-A	CH30-B	CH30-C	CH30-D	CH29-A	CH29-B	CH29-C	CH29-D	TS16

Register Name: **TS1 to TS16**
Register Description: **Transmit Signaling Registers (E1 Mode, CCS Format)**
Register Address: **50h to 5Fh**

(MSB)							(LSB)	
1	2	3	4	5	6	7	8	TS1
17	18	19	20	9	10	11	12	TS2
33	34	35	36	25	26	27	28	TS3
49	50	51	52	41	42	43	44	TS4
65	66	67	68	57	58	59	60	TS5
81	82	83	84	73	74	75	76	TS6
97	98	99	100	89	90	91	92	TS7
113	114	115	116	105	106	107	108	TS8
13	14	15	16	121	122	123	124	TS9
29	30	31	32	21	22	23	24	TS10
45	46	47	48	37	38	39	40	TS11
61	62	63	64	53	54	55	56	TS12
77	78	89	80	69	70	71	72	TS13
93	94	95	96	85	86	87	88	TS14
109	110	111	112	101	102	103	104	TS15
125	126	127	128	117	118	119	120	TS16

Register Name: **TS1 to TS16**
Register Description: **Transmit Signaling Registers (T1 Mode, ESF Format)**
Register Address: **50h to 5Bh**

(MSB)							(LSB)	
CH2-A	CH2-B	CH2-C	CH2-D	CH1-A	CH1-B	CH1-C	CH1-D	TS1
CH4-A	CH4-B	CH4-C	CH4-D	CH3-A	CH3-B	CH3-C	CH3-D	TS2
CH6-A	CH6-B	CH6-C	CH6-D	CH5-A	CH5-B	CH5-C	CH5-D	TS3
CH8-A	CH8-B	CH8-C	CH8-D	CH7-A	CH7-B	CH7-C	CH7-D	TS4
CH10-A	CH10-B	CH10-C	CH10-D	CH9-A	CH9-B	CH9-C	CH9-D	TS5
CH12-A	CH12-B	CH12-C	CH12-D	CH11-A	CH11-B	CH11-C	CH11-D	TS6
CH14-A	CH14-B	CH14-C	CH14-D	CH13-A	CH13-B	CH13-C	CH13-D	TS7
CH16-A	CH16-B	CH16-C	CH16-D	CH15-A	CH15-B	CH15-C	CH15-D	TS8
CH18-A	CH18-B	CH18-C	CH18-D	CH17-A	CH17-B	CH17-C	CH17-D	TS9
CH20-A	CH20-B	CH20-C	CH20-D	CH19-A	CH19-B	CH19-C	CH19-D	TS10
CH22-A	CH22-B	CH22-C	CH22-D	CH21-A	CH21-B	CH21-C	CH21-D	TS11
CH24-A	CH24-B	CH24-C	CH24-D	CH23-A	CH23-B	CH23-C	CH23-D	TS12

Register Name: **TS1 to TS16**
Register Description: **Transmit Signaling Registers (T1 Mode, D4 Format)**
Register Address: **50h to 5Bh**

(MSB)							(LSB)	
CH2-A	CH2-B	**CH2-A**	**CH2-B**	CH1-A	CH1-B	**CH1-A**	**CH1-B**	TS1
CH4-A	CH4-B	**CH4-A**	**CH4-B**	CH3-A	CH3-B	**CH3-A**	**CH3-B**	TS2
CH6-A	CH6-B	**CH6-A**	**CH6-B**	CH5-A	CH5-B	**CH5-A**	**CH5-B**	TS3
CH8-A	CH8-B	**CH8-A**	**CH8-B**	CH7-A	CH7-B	**CH7-A**	**CH7-B**	TS4
CH10-A	CH10-B	**CH10-A**	**CH10-B**	CH9-A	CH9-B	**CH9-A**	**CH9-B**	TS5
CH12-A	CH12-B	**CH12-A**	**CH12-B**	CH11-A	CH11-B	**CH11-A**	**CH11-B**	TS6
CH14-A	CH14-B	**CH14-A**	**CH14-B**	CH13-A	CH13-B	**CH13-A**	**CH13-B**	TS7
CH16-A	CH16-B	**CH16-A**	**CH16-B**	CH15-A	CH15-B	**CH15-A**	**CH15-B**	TS8
CH18-A	CH18-B	**CH18-A**	**CH18-B**	CH17-A	CH17-B	**CH17-A**	**CH17-B**	TS9
CH20-A	CH20-B	**CH20-A**	**CH20-B**	CH19-A	CH19-B	**CH19-A**	**CH19-B**	TS10
CH22-A	CH22-B	**CH22-A**	**CH22-B**	CH21-A	CH21-B	**CH21-A**	**CH21-B**	TS11
CH24-A	CH24-B	**CH24-A**	**CH24-B**	CH23-A	CH23-B	**CH23-A**	**CH23-B**	TS12

Note: In D4 format, TS1–TS12 contain signaling data for two frames. Bold type indicates data for second frame.

15.2.2 Software Signaling Insertion Enable Registers, E1 CAS Mode

In E1 CAS mode, the CAS signaling alignment/alarm byte can be sourced from the transmit signaling registers along with the signaling data.

Register Name: **SSIE1**
Register Description: **Software Signaling Insertion Enable 1**
Register Address: **08h**

Bit #	7	6	5	4	3	2	1	0
Name	CH7	CH6	CH5	CH4	CH3	CH2	CH1	UCAW
Default	0	0	0	0	0	0	0	0

Bit 0/Upper CAS Align/Alarm Word (UCAW). Selects the upper CAS align/alarm pattern (0000) to be sourced from the upper 4 bits of the TS1 register.

0 = do not source the upper CAS align/alarm pattern from the TS1 register
1 = source the upper CAS align/alarm pattern from the TS1 register

Bits 1 to 7/Software Signaling Insertion Enable for Channels 1 to 7 (CH1 to CH7). These bits determine which channels are to have signaling inserted form the Transmit Signaling registers.

0 = do not source signaling data from the TSx registers for this channel
1 = source signaling data from the TSx registers for this channel

Register Name: **SSIE2**
Register Description: **Software Signaling Insertion Enable 2**
Register Address: **09h**

Bit #	7	6	5	4	3	2	1	0
Name	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Software Signaling Insertion Enable for Channels 8 to 15 (CH8 to CH15). These bits determine which channels are to have signaling inserted form the transmit signaling registers.

0 = do not source signaling data from the TS registers for this channel
1 = source signaling data from the TS registers for this channel

Register Name: **SSIE3**
Register Description: **Software Signaling Insertion Enable 3**
Register Address: **0Ah**

Bit #	7	6	5	4	3	2	1	0
Name	CH22	CH21	CH20	CH19	CH18	CH17	CH16	LCAW
Default	0	0	0	0	0	0	0	0

Bit 0/Lower CAS Align/Alarm Word (LCAW). Selects the lower CAS align/alarm bits (xyxx) to be sourced from the lower 4 bits of the TS1 register.

0 = do not source the lower CAS align/alarm bits from the TS1 register
1 = source the lower CAS alarm align/bits from the TS1 register

Bits 1 to 7/Software Signaling Insertion Enable for LCAW and Channels 16 to 22 (CH16 to CH22). These bits determine which channels are to have signaling inserted form the Transmit Signaling registers.

0 = do not source signaling data from the TSx regis ters for this channel
1 = source signaling data from the TSx registers for this channel

Register Name: **SSIE4**
Register Description: **Software Signaling Insertion Enable 4**
Register Address: **0Bh**

Bit #	7	6	5	4	3	2	1	0
Name	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Software Signaling Insertion Enable for Channels 23 to 30 (CH23 to CH30). These bits determine which channels are to have signaling inserted form the transmit signaling registers.

0 = do not source signaling data from the TS registers for this channel
1 = source signaling data from the TS registers for this channel

15.2.3 Software Signaling Insertion Enable Registers, T1 Mode

In T1 mode, only registers SSIE1 through SSIE3 are used since there are only 24 channels in a T1 frame.

Register Name: **SSIE1**
Register Description: **Software Signaling Insertion Enable 1**
Register Address: **08h**

Bit #	7	6	5	4	3	2	1	0
Name	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Software Signaling Insertion Enable for and Channels 1 to 8 (CH1 to CH8). These bits determine what channels are to have signaling inserted form the transmit signaling registers.

0 = do not source signaling data from the TSx registers for this channel
1 = source signaling data from the TSx registers for this channel

Register Name: **SSIE2**
Register Description: **Software Signaling Insertion Enable 2**
Register Address: **09h**

Bit #	7	6	5	4	3	2	1	0
Name	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Software Signaling Insertion Enable for Channels 9 to 16 (CH9 to CH16). These bits determine what channels are to have signaling inserted form the transmit signaling registers.

0 = do not source signaling data from the TSx registers for this channel
1 = source signaling data from the TSx registers for this channel

Register Name: **SSIE3**
Register Description: **Software Signaling Insertion Enable 3**
Register Address: **0Ah**

Bit #	7	6	5	4	3	2	1	0
Name	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Software Signaling Insertion Enable for and Channels 17 to 24 (CH17 to CH24). These bits determine what channels are to have signaling inserted form the transmit signaling registers.

0 = do not source signaling data from the TSx registers for this channel
1 = source signaling data from the TSx registers for this channel

17.2.4 Hardware-Based Transmit Signaling

In hardware-based mode, signaling data is input via the TSIG pin. This signaling PCM stream is buffered and inserted to the data stream being input at the TSER pin.

Signaling data can be input on a per-channel basis via the transmit-hardware signaling-channel select (THSCS) function. The framer can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The user has the ability to control what channels are to have signaling data from the TSIG pin inserted into them on a per-channel basis. See the *Special Per-Channel Operation* section. The signaling insertion capabilities of the framer are available whether the transmit side elastic store is enabled or disabled. If the elastic store is enabled, the backplane clock (TSYSCLK) can be either 1.544MHz or 2.048MHz.

16. PER-CHANNEL IDLE CODE GENERATION

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. When operated in the T1 mode, only the first 24 channels are used; the remaining channels, CH25–CH32 are not used.

The DS21Q55 contains a 64-byte idle code array accessed by the idle array address register (IAAR) and the per-channel idle code register (PCICR). The contents of the array contain the idle codes to be substituted into the appropriate transmit or receive channels. This substitution can be enabled and disabled on a per-channel basis by the transmit-channel idle-code enable registers (TCICE1–4) and receive-channel idle-code enable registers (RCICE1–4).

To program idle codes, first select a channel by writing to the IAAR register. Then write the idle code to the PCICR register. For successive writes there is no need to load the IAAR with the next consecutive address. The IAAR register will automatically increment after a write to the PCICR register. The auto increment feature can be used for read operations as well.

Bits 6 and 7 (GTIC, GRIC) of the IAAR register can be used to block write a common idle code to all transmit or receive positions in the array with a single write to the PCICR register. The user can use the block write feature to set a common idle code for all transmit and receive channels in the IAAR by setting both GTIC and GRIC = 1. When a block write is enabled by GTIC or GRIC, the value placed in the PCICR register will be written to all addresses in the transmit or receive idle array and to whatever address is in the lower 6 bits of the IAAR register. Therefore, when enabling only one of the block functions, GTIC or GRIC, the user must set the lower 6 bits of the IAAR register to any address in that block. Bits 6 and 7 of the IAAR register must be set = 0 for read operations.

The TCICE1–4 and RCICE1–4 are used to enable idle-code replacement on a per-channel basis.

IDLE CODE ARRAY ADDRESS MAPPING Table 18-1

BITS 0–5 OF IAAR REGISTER	MAPS TO CHANNEL
0	Transmit Channel 1
1	Transmit Channel 2
2	Transmit Channel 3
-	
-	
30	Transmit Channel 31
31	Transmit Channel 32
32	Receive Channel 1
33	Receive Channel 2
34	Receive Channel 3
-	
-	
62	Receive Channel 31
63	Receive Channel 32

16.1 Idle Code Programming Examples

The following example sets transmit channel 3 idle code to 7Eh:

```
Write IAAR = 02h      ;select channel 3 in the array
Write PCICR = 7Eh     ;set idle code to 7Eh
```

The following example sets transmit channels 3, 4, 5, and 6 idle code to 7Eh and enables transmission of idle codes for those channels:

```
Write IAAR = 02h      ;select channel 3 in the array
Write PCICR = 7Eh     ;set channel 3 idle code to 7Eh
Write PCICR = 7Eh     ;set channel 4 idle code to 7Eh
Write PCICR = 7Eh     ;set channel 5 idle code to 7Eh
Write PCICR = 7Eh     ;set channel 6 idle code to 7Eh
Write TCICE1 = 3Ch    ;enable transmission of idle codes for channels 3, 4, 5, and 6
```

The following example sets transmit channels 3, 4, 5, and 6 idle code to 7Eh, EEh, FFh, and 7Eh respectively:

```
Write IAAR = 02h
Write PCICR = 7Eh
Write PCICR = EEh
Write PCICR = FFh
Write PCICR = 7Eh
```

The following example sets all transmit idle codes to 7Eh:

```
Write IAAR = 40h
Write PCICR = 7Eh
```

The following example sets all receive and transmit idle codes to 7Eh and enables idle code substitution in all E1 transmit and receive channels:

```
Write IAAR = C0h      ;enable block write to all transmit and receive positions in the array
Write PCICR = 7Eh     ;7Eh is idle code
Write TCICE1 = FEh    ;enable idle code substitution for transmit channels 2 through 8
                      ;Although an idle code was programmed for channel 1 by the block write ;function above,
                      enabling it for channel 1 would step on the frame ;alignment, alarms, and Sa bits
Write TCICE2 = FFh    ;enable idle code substitution for transmit channels 9 through 16
Write TCICE3 = FEh    ;enable idle code substitution for transmit channels 18 through 24
                      ;Although an idle code was programmed for channel 17 by the block write ;function above,
                      enabling it for channel 17 would step on the CAS frame ;alignment, and signaling information
Write TCICE4 = FFh    ;enable idle code substitution for transmit channels 25 through 32
Write RCICE1 = FEh    ;enable idle code substitution for receive channels 2 through 8
Write RCICE2 = FFh    ;enable idle code substitution for receive channels 9 through 16
Write RCICE3 = FEh    ;enable idle code substitution for receive channels 18 through 24
Write RCICE4 = FFh    ;enable idle code substitution for receive channels 25 through 32
```

Register Name: **IAAR**
Register Description: **Idle Array Address Register**
Register Address: **7Eh**

Bit #	7	6	5	4	3	2	1	0
Name	GRIC	GTIC	IAA5	IAA4	IAA3	IAA2	IAA1	IAA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 5/Channel Pointer Address Bits (IAA0 to IAA5). IAA0 is the LSB of the 5-bit Channel Code.

Bit 6/Global Transmit Idle Code (GTIC). Setting this bit will cause all transmit idle codes to be set to the value written to the PCICR register. When using this bit, the user must place any transmit address in the IAA0 through IAA5 bits (00h–1Fh). This bit must be set = 0 for read operations.

Bit 7/Global Receive Idle Code (GRIC). Setting this bit will cause all receive idle codes to be set to the value written to the PCICR register. When using this bit, the user must place any receive address in the IAA0 through IAA5 bits (20h–3Fh). This bit must be set = 0 for read operations.

Register Name: **PCICR**
Register Description: **Per-Channel Idle Code Register**
Register Address: **7Fh**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Per-Channel Idle Code Bits (C0 to C7). C0 is the LSB of the code (this bit is transmitted last).

The TCICE1/2/3/4 are used to determine which of the 24 T1 or 32 E1 channels from the backplane to the T1 or E1 line should be overwritten with the code placed in the per-channel code array.

Register Name: **TCICE1**
Register Description: **Transmit Channel Idle Code Enable Register 1**
Register Address: **80h**

Bit #	7	6	5	4	3	2	1	0
Name	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 1 to 8 Code Insertion Control Bits (CH1 to CH8).
0 = do not insert data from the idle code array into the transmit data stream
1 = insert data from the idle code array into the transmit data stream

Register Name: **TCICE2**
Register Description: **Transmit Channel Idle Code Enable Register 2**
Register Address: **81h**

Bit #	7	6	5	4	3	2	1	0
Name	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 9 to 16 Code Insertion Control Bits (CH9 to CH16).
0 = do not insert data from the idle code array into the transmit data stream

1 = insert data from the idle code array into the transmit data stream

Register Name: **TCICE3**
Register Description: **Transmit Channel Idle Code Enable Register 3**
Register Address: **82h**

Bit #	7	6	5	4	3	2	1	0
Name	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 17 to 24 Code Insertion Control Bits (CH17 to CH24).
0 = do not insert data from the idle code array into the transmit data stream
1 = insert data from the idle code array into the transmit data stream

Register Name: **TCICE4**
Register Description: **Transmit Channel Idle Code Enable Register 4**
Register Address: **83h**

Bit #	7	6	5	4	3	2	1	0
Name	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 25 to 32 Code Insertion Control Bits (CH25 to CH32).
0 = do not insert data from the idle code array into the transmit data stream
1 = insert data from the idle code array into the transmit data stream

The receive-channel idle-code enable registers (RCICE1/2/3/4) are used to determine which of the 24 T1 or 32 E1 channels from the backplane to the T1 or E1 line should be overwritten with the code placed in the per-channel code array.

Register Name: **RCICE1**
Register Description: **Receive Channel Idle Code Enable Register 1**
Register Address: **84h**

Bit #	7	6	5	4	3	2	1	0
Name	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 1 to 8 Code Insertion Control Bits (CH1 to CH8).
0 = do not insert data from the idle code array into the receive data stream
1 = insert data from the idle code array into the receive data stream

Register Name: **RCICE2**
Register Description: **Receive Channel Idle Code Enable Register 2**
Register Address: **85h**

Bit #	7	6	5	4	3	2	1	0
Name	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 9 to 16 Code Insertion Control Bits (CH9 to CH16).
0 = do not insert data from the idle code array into the receive data stream
1 = insert data from the idle code array into the receive data stream

Register Name: **RCICE3**
Register Description: **Receive Channel Idle Code Enable Register 3**
Register Address: **86h**

Bit #	7	6	5	4	3	2	1	0
Name	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 17 to 24 Code Insertion Control Bits (CH17 to CH24).
0 = do not insert data from the idle code array into the receive data stream
1 = insert data from the idle code array into the receive data stream

Register Name: **RCICE4**
Register Description: **Receive Channel Idle Code Enable Register 4**
Register Address: **87h**

Bit #	7	6	5	4	3	2	1	0
Name	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 25 to 32 Code Insertion Control Bits (CH25 to CH32).
0 = do not insert data from the idle code array into the receive data stream
1 = insert data from the idle code array into the receive data stream

17. CHANNEL BLOCKING REGISTERS

The receive-channel blocking registers (RCBR1/RCBR2/RCBR3/RCBR4) and the transmit-channel blocking registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins, respectively. The RCHBLK and TCHBLK pins are user-programmable outputs that can be forced high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN–PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHBLK pin will be held high during the entire corresponding channel time. Channels 25 through 32 are ignored when the device is operated in the T1 mode.

Also, the DS21Q55 can internally generate and output a bursty clock on a per-channel basis (N x 64kbps / 56kbps). See *Fractional T1/E1 Support*.

Register Name: **RCBR1**
Register Description: **Receive Channel Blocking Register 1**
Register Address: **88h**

Bit #	7	6	5	4	3	2	1	0
Name	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 1 to 8 Channel Blocking Control Bits (CH1 to CH8).
0 = force the RCHBLK pin to remain low during this channel time
1 = force the RCHBLK pin high during this channel time

Register Name: **RCBR2**
Register Description: **Receive Channel Blocking Register 2**
Register Address: **89h**

Bit #	7	6	5	4	3	2	1	0
Name	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 9 to 16 Channel Blocking Control Bits (CH9 to CH16).
0 = force the RCHBLK pin to remain low during this channel time
1 = force the RCHBLK pin high during this channel time

Register Name: **RCBR3**
Register Description: **Receive Channel Blocking Register 3**
Register Address: **8Ah**

Bit #	7	6	5	4	3	2	1	0
Name	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 17 to 24 Channel Blocking Control Bits (CH17 to CH24).
0 = force the RCHBLK pin to remain low during this channel time
1 = force the RCHBLK pin high during this channel time

Register Name: **RCBR4**
Register Description: **Receive Channel Blocking Register 4**
Register Address: **8Bh**

Bit #	7	6	5	4	3	2	1	0
Name	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Receive Channels 25 to 32 Channel Blocking Control Bits (CH25 to CH32).
0 = force the RCHBLK pin to remain low during this channel time
1 = force the RCHBLK pin high during this channel time

Register Name: **TCBR1**
Register Description: **Transmit Channel Blocking Register 1**
Register Address: **8Ch**

Bit #	7	6	5	4	3	2	1	0
Name	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 1 to 8 Channel Blocking Control Bits (CH1 to CH8).
0 = force the TCHBLK pin to remain low during this channel time
1 = force the TCHBLK pin high during this channel time

Register Name: **TCBR2**
Register Description: **Transmit Channel Blocking Register 2**
Register Address: **8Dh**

Bit #	7	6	5	4	3	2	1	0
Name	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 9 to 16 Channel Blocking Control Bits (CH9 to CH16).
0 = force the TCHBLK pin to remain low during this channel time
1 = force the TCHBLK pin high during this channel time

Register Name: **TCBR3**
Register Description: **Transmit Channel Blocking Register 3**
Register Address: **8Eh**

Bit #	7	6	5	4	3	2	1	0
Name	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 17 to 24 Channel Blocking Control Bits (CH17 to CH24).
0 = force the TCHBLK pin to remain low during this channel time
1 = force the TCHBLK pin high during this channel time

Register Name: **TCBR4**
Register Description: **Transmit Channel Blocking Register 4**
Register Address: **8Fh**

Bit #	7	6	5	4	3	2	1	0
Name	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit Channels 25 to 32 Channel Blocking Control Bits (CH25 to CH32).
0 = force the TCHBLK pin to remain low during this channel time
1 = force the TCHBLK pin high during this channel time

18. ELASTIC STORES OPERATION

The DS21Q55 contains dual two-frame, fully independent elastic stores, one for the receive direction and one for the transmit direction. The transmit- and receive-side elastic stores can be enabled/disabled independent of each other. Also, each elastic store can interface to either a 1.544MHz or 2.048MHz/4.096MHz/8.192MHz/16.384MHz backplane without regard to the backplane rate the other elastic store is interfacing to.

The elastic stores have two main purposes. First, they can be used for rate conversion. When the device is in the T1 mode, the elastic stores can rate-convert the T1 data stream to a 2.048MHz backplane. In E1 mode, the elastic store can rate-convert the E1 data stream to a 1.544MHz backplane. Second, they can be used to absorb the differences in frequency and phase between the T1 or E1 data stream and an asynchronous (not locked) backplane clock (which can be 1.544MHz or 2.048MHz). In this mode, the elastic stores will manage the rate difference and perform controlled slips, deleting or repeating frames of data in order to manage the difference between the network and the backplane.

The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates. See *Interleaved PCM Bus Operation.*

Register Name: **ESCR**
Register Description: **Elastic Store Control Register**
Register Address: **4Fh**

Bit #	7	6	5	4	3	2	1	0
Name	TESALGN	TESR	TESMDM	TESE	RESALGN	RESR	RESMDM	RESE
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Elastic Store Enable (RESE).
0 = elastic store is bypassed
1 = elastic store is enabled

Bit 1/Receive Elastic Store Minimum Delay Mode (RESMDM). See *Minimum Delay Mode.*
0 = elastic stores operate at full two frame depth
1 = elastic stores operate at 32–bit depth

Bit 2/Receive Elastic Store Reset (RESR). Setting this bit from a zero to a one forces the read and write pointers into opposite frames, maximizing the delay through the receive elastic store. Should be toggled after RSYSCLK has been applied and is stable. See *Elastic Stores Initialization* for details. Do not leave this bit set HIGH.

Bit 3/Receive Elastic Store Align (RESALGN). Setting this bit from a zero to a one will force the receive elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after RSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See *Elastic Stores Initialization* for details.

Bit 4/Transmit Elastic Store Enable (TESE).
0 = elastic store is bypassed
1 = elastic store is enabled

Bit 5/Transmit Elastic Store Minimum Delay Mode (TESMDM). See *Minimum Delay Mode* for details.
0 = elastic stores operate at full two frame depth
1 = elastic stores operate at 32-bit depth

Bit 6/Transmit Elastic Store Reset (TESR). Setting this bit from a zero to a one forces the read and write pointers into opposite frames, maximizing the delay through the transmit elastic store. Transmit data is lost during the reset. Should be toggled after TSYSCLK has been applied and is stable. See *Elastic Stores Initialization* for details. Do not leave this bit set HIGH.

Bit 7/Transmit Elastic Store Align (TESALGN). Setting this bit from a zero to a one will force the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after TSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See *Elastic Stores Initialization* for details.

Register Name: **SR5**
Register Description: **Status Register 5**
Register Address: **1Eh**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	TESF	TESEM	TSLIP	RESF	RESEM	RSLIP
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Elastic Store Slip Occurrence Event (RSLIP). Set when the receive elastic store has either repeated or deleted a frame.

Bit 1/Receive Elastic Store Empty Event (RESEM). Set when the receive elastic store buffer empties and a frame is repeated.

Bit 2/Receive Elastic Store Full Event (RESF). Set when the receive elastic store buffer fills and a frame is deleted.

Bit 3/Transmit Elastic Store Slip Occurrence Event (TSLIP). Set when the transmit elastic store has either repeated or deleted a frame.

Bit 4/Transmit Elastic Store Empty Event (TESEM). Set when the transmit elastic store buffer empties and a frame is repeated.

Bit 5/Transmit Elastic Store Full Event (TESF). Set when the transmit elastic store buffer fills and a frame is deleted.

Register Name: **IMR5**
Register Description: **Interrupt Mask Register 5**
Register Address: **1Fh**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	TESF	TESEM	TSLIP	RESF	RESEM	RSLIP
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Elastic Store Slip Occurrence Event (RSLIP).
0 = interrupt masked
1 = interrupt enabled

Bit 1/Receive Elastic Store Empty Event (RESEM).
0 = interrupt masked
1 = interrupt enabled

Bit 2/Receive Elastic Store Full Event (RESF).
0 = interrupt masked
1 = interrupt enabled

Bit 3/Transmit Elastic Store Slip Occurrence Event (TSLIP).
0 = interrupt masked
1 = interrupt enabled

Bit 4/Transmit Elastic Store Empty Event (TESEM).
0 = interrupt masked
1 = interrupt enabled

Bit 5/Transmit Elastic Store Full Event (TESF).
0 = interrupt masked
1 = interrupt enabled

18.1 Receive Side

See the IOCR1 and IOCR2 registers for information on clock and I/O configurations.

If the receive-side elastic store is enabled, then the user must provide either a 1.544MHz or 2.048MHz clock at the RSYSCLK pin. For higher rate system-clock applications, see the *Interleaved PCM Bus Operation* section. The user has the option of either providing a frame/multiframe sync at the RSYNC pin or having the RSYNC pin provide a pulse on frame/multiframe boundaries. If signaling reinsertion is enabled, signaling data in TS16 is realigned to the multiframe-sync input on RSYNC. Otherwise, a multiframe-sync input on RSYNC is treated as a simple frame boundary by the elastic store. The framer will always indicate frame boundaries on the network side of the elastic store via the RFSYNC output whether the elastic store is enabled or not. Multiframe boundaries will always be indicated via the RMSYNC output. If the elastic store is enabled, then RMSYNC will output the multiframe boundary on the backplane side of the elastic store.

18.1.1 T1 Mode

If the user selects to apply a 2.048MHz clock to the RSYSCLK pin, then the data output at RSER will be forced to all ones every fourth channel and the F-bit will be passed into the MSB of TS0. Hence, channels 1 (bits 1–7), 5, 9, 13, 17, 21, 25, and 29 (timeslots 0 (bits 1-7), 4, 8, 12, 16, 20, 24, and 28) will be forced to a one. Also, in 2.048MHz applications, the RCHBLK output will be forced high during the same channels as the RSER pin. This is useful in T1 to E1 conversion applications. If the two-frame elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data will be repeated at RSER and the SR5.0 and SR5.1 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR5.0 and SR5.2 bits will be set to a one.

18.1.2 E1 Mode

If the elastic store is enabled, then either CAS or CRC4 multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 1.544MHz clock to the RSYSCLK pin, then every fourth channel of the received E1 data will be deleted and a F-bit position (which will be forced to one) will be inserted. Hence, channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted from the received E1 data stream. Also, in 1.544MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). If the two-frame elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data will be repeated at RSER and the SR5.0 and SR5.1 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR5.0 and SR5.2 bits will be set to a one.

18.2 Transmit Side

See the IOCR1 and IOCR2 registers for information on clock and I/O configurations.

The operation of the transmit elastic store is very similar to the receive side. If the transmit-side elastic store is enabled a 1.544MHz or 2.048MHz clock can be applied to the TSYSCLK input. For higher rate system-clock applications, see the *Interleaved PCM Bus Operation* section. Controlled slips in the transmit elastic store are reported in the SR5.3 bit and the direction of the slip is reported in the SR5.4 and SR5.5 bits.

18.2.1 T1 Mode

If the user selects to apply a 2.048MHz clock to the TSYSCLK pin, then the data input at TSER will be ignored every fourth channel. Hence, channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be ignored. The user can supply frame or multiframe sync pulse to the TSSYNC input. Also, in 2.048MHz applications, the TCHBLK output will be forced high during the channels ignored by the framer.

18.2.2 E1 Mode

A 1.544MHz or 2.048MHz clock can be applied to the TSYSCLK input. The user must supply a frame-sync pulse or a multiframe-sync pulse to the TSSYNC input.

18.3 Elastic Stores Initialization

There are two elastic-store initializations that can be used to improve performance in certain applications, elastic store reset and elastic store align. Both of these involve the manipulation of the elastic store's read and write pointers and are useful primarily in synchronous applications (RSYSCLK/TSYSCLK are locked to RCLK/TCLK, respectively). See table below for details.

ELASTIC STORE DELAY AFTER INITIALIZATION Table 20-1

INITIALIZATION	REGISTER BIT	DELAY
Receive Elastic Store Reset	ESCR.2	8 Clocks < Delay < 1 Frame
Transmit Elastic Store Reset	ESCR.6	1 Frame < Delay < 2 Frames
Receive Elastic Store Align	ESCR.3	½ Frame < Delay < 1 ½ Frames
Transmit Elastic Store Align	ESCR.7	½ Frame < Delay < 1 ½ Frames

18.4 Minimum-Delay Mode

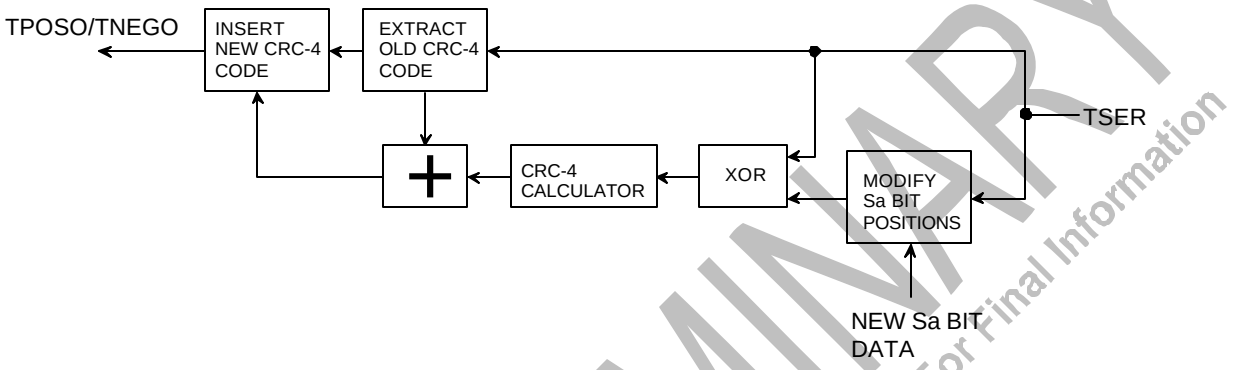
Elastic store minimum-delay mode can be used when the elastic store's system clock is locked to its network clock (e.g., RCLK locked to RSYSCLK for the receive side and TCLK locked to TSYSCLK for the transmit side). ESCR.5 and ESCR.1 enable the transmit and receive elastic store minimum-delay modes. When enabled the elastic stores will be forced to a maximum depth of 32 bits instead of the normal two-frame depth. This feature is useful primarily in applications that interface to a 2.048MHz bus. Certain restrictions apply when minimum delay mode is used. In addition to the restriction mentioned above, RSYNC must be configured as an output when the receive elastic store is in minimum delay mode and TSYNC must be configured as an output when transmit minimum delay mode is enabled. In a typical application RSYSCLK and TSYSCLK are locked to RCLK, and RSYNC (frame output mode) is connected to TSSYNC (frame input mode). All of the slip contention logic in the framer is disabled (since slips cannot occur). On power-up, after the RSYSCLK and TSYSCLK signals have locked to their

respective network clock signals, the elastic store reset bits (ESCR.2 and ESCR.6) should be toggled from a zero to a one to ensure proper operation.

19. G.706 INTERMEDIATE CRC-4 UPDATING (E1 MODE ONLY)

The DS21Q55 can implement the G.706 CRC-4 recalculation at intermediate path points. When this mode is enabled, the data stream presented at TSER will already have the FAS/NFAS, CRC multiframe alignment word, and CRC-4 checksum in timeslot 0. The user can modify the Sa bit positions; this change in data content will be used to modify the CRC-4 checksum. The modification, however, will not corrupt any error information the original CRC-4 checksum might contain. In this mode of operation, TSYNC must be configured to multiframe mode. The data at TSER must be aligned to the TSYNC signal. If TSYNC is an input then the user must assert TSYNC aligned at the beginning of the multiframe relative to TSER. If TSYNC is an output, the user must multiframe-align the data presented to TSER.

CRC-4 RECALCULATE METHOD Figure 21-1



20. T1 BIT ORIENTED CODE (BOC) CONTROLLER

The DS21Q55 contains a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1 mode.

20.1 Transmit BOC

Bits 0 through 5 in the TFDL register contain the BOC message to be transmitted. Setting BOCC.0 = 1 causes the transmit BOC controller to immediately begin inserting the BOC sequence into the FDL bit position. The transmit BOC controller automatically provides the abort sequence. BOC messages will be transmitted as long as BOCC.0 is set.

To transmit a BOC, use the following:

1) Write 6-bit code into the TFDL register.
2) Set SBOC bit in BOCC register = 1.

20.2 Receive BOC

The receive BOC function is enabled by setting BOCC.4 = 1. The RFDL register will now operate as the receive BOC message and information register. The lower six bits of the RFDL register (BOC message bits) are preset to all ones. When the BOC bits change state, the BOC change of state indicator, SR8.0 will alert the host. The host will then read the RFDL register to get the BOC message. A change of state will occur when either a new BOC code has been present for time determined by the receive BOC filter bits, RBF0 and RBF1, in the BOCC register.

To receive a BOC, use the following:

1) Set integration time via BOCC.1 and BOCC.2.
2) Enable the receive BOC function (BOCC.4 = 1).
3) Enable interrupt (IMR8.0 = 1).
4) Wait for interrupt to occur.
5) Read the RFDL register.
6) The lower six bits of the RFDL register is the message.

Register Name: **BOCC**
Register Description: **BOC Control Register**
Register Address: **37h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	RBOCE	RBR	RBF1	RBF0	SBOC
Default	0	0	0	0	0	0	0	0

Bit 0/Send BOC (SBOC). Set = 1 to transmit the BOC code placed in bits 0 to 5 of the TFDL register.

Bits 1 to 2/Receive BOC Filter Bits (RBF0, RBF1). The BOC filter sets the number of consecutive patterns that must be received without error prior to an indication of a valid message.

RBF1	RBF0	CONSECUTIVE BOC CODES FOR VALID SEQUENCE IDENTIFICATION
0	0	None
0	1	3
1	0	5
1	1	7

Bit 3/Receive BOC Reset (RBR). A 0 to 1 transition will reset the BOC circuitry. Must be cleared and set again for a subsequent reset.

Bit 4/Receive BOC Enable (RBOCE). Enables the receive BOC function. The RFDL register will report the received BOC code.

0 = receive BOC function disabled
1 = receive BOC function enabled. The RFDL register will report BOC messages

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **RFDL** (RFDL register bit usage when BOCC.4 = 1)
Register Description: **Receive FDL Register**
Register Address: **C0h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	RBOC5	RBOC4	RBOC3	RBOC2	RBOC1	RBOC0
Default	0	0	0	0	0	0	0	0

Bit 0/BOC Bit 0 (RBOC0).

Bit 1/BOC Bit 1 (RBOC1).

Bit 2/BOC Bit 2 (RBOC2).

Bit 3/BOC Bit 3 (RBOC3).

Bit 4/BOC Bit 4 (RBOC4).

Bit 5/BOC Bit 5 (RBOC5).

Bit 6/This bit position is unused when BOCC.4 = 1.

Bit 7/This bit position is unused when BOCC.4 = 1.

Register Name: **SR8**
Register Description: **Status Register 8**
Register Address: **24h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	BOCC	RFDLAD	RFDLF	TFDLE	RMTCH	RBOC
Default	0	0	0	0	0	0	0	0

Bit 0/Receive BOC Detector Change of State Event (RBOC). Set whenever the BOC detector sees a change of state to a valid BOC. The setting of this bit prompts the user to read the RFDL register.

Bit 1/Receive FDL Match Event (RMTCH). Set whenever the contents of the RFDL register matches RFDLM1 or RFDLM2.

Bit 2/TFDL Register Empty Event(TFDLE). Set when the transmit FDL buffer (TFDL) empties.

Bit 3/RFDL Register Full Event (RFDLF). Set when the receive FDL buffer (RFDL) fills to capacity.

Bit 4/RFDL Abort Detect Event (RFDLAD). Set when eight consecutive ones are received on the FDL.

Bit 5/BOC Clear Event (BOCC). Set when 30 FDL bits occur without an abort sequence.

Register Name: **IMR8**
Register Description: **Interrupt Mask Register 8**
Register Address: **25h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	BOCC	RFDLAD	RFDLF	TFDLE	RMTCH	RBOC
Default	0	0	0	0	0	0	0	0

Bit 0/Receive BOC Detector Change of State Event (RBOC).
0 = interrupt masked
1 = interrupt enabled

Bit 1/Receive FDL Match Event (RMTCH).
0 = interrupt masked
1 = interrupt enabled

Bit 2/TFDL Register Empty Event (TFDLE).
0 = interrupt masked
1 = interrupt enabled

Bit 3/RFDL Register Full Event (RFDLF).
0 = interrupt masked
1 = interrupt enabled

Bit 4/RFDL Abort Detect Event (RFDLAD).
0 = interrupt masked
1 = interrupt enabled

Bit 5/BOC Clear Event (BOCC).
0 = interrupt masked
1 = interrupt enabled

21. ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION (E1 ONLY)

The DS21Q55, when operated in the E1 mode, provides for access to both the Sa and the Si bits via three different methods. The first method is via a hardware scheme using the RLINK/RLCLK and TLINK/TLCLK pins. The second method involves using the internal RAF/RNAF and TAF/TNAF registers. The third method involves an expanded version of the second method.

21.1 Hardware Scheme (Method 1)

On the receive side, all of the received data is reported at the RLINK pin. Using the E1RCR2 register the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits. If RSYNC is programmed to output a frame boundary, it will identify the Si bits.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register or externally from the TLINK pin. Using the E1TCR2 register the framer can be programmed to source any combination of the Sa bits from the TLINK pin. Si bits can be sampled through the TSER pin if by setting E1TCR1.4 = 0.

21.2 Internal Register Scheme Based On Double-Frame (Method 2)

On the receive side, the RAF and RNAF registers will always report the data as it received in the Sa and Si bit locations. The RAF and RNAF registers are updated on align frame boundaries. The setting of the receive align frame bit in status register 4 (SR4.0) will indicate that the contents of the RAF and RNAF have been updated. The host can use the SR4.0 bit to know when to read the RAF and RNAF registers. The host has 250µs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the transmit align frame bit in status register 4 (SR4.3). The host can use the SR4.3 bit to know when to update the TAF and TNAF registers. It has 250µs to update the data or else the old data will be retransmitted**. If the TAF an TNAF registers are only being used to source the align frame and nonalign frame-sync patterns, then the host need only write once to these registers**. Data in the Si bit position will be overwritten if the framer is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) with automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the E1TCR2.3 to E1TCR2.7 bits are set to one.

Register Name: **RAF**
Register Description: **Receive Align Frame Register**
Register Address: **C6h**

Bit #	7	6	5	4	3	2	1	0
Name	Si	0	0	1	1	0	1	1
Default	0	0	0	0	0	0	0	0

Bit 0/Frame Alignment Signal Bit (1).

Bit 1/Frame Alignment Signal Bit (1).

Bit 2/Frame Alignment Signal Bit (0).

Bit 3/Frame Alignment Signal Bit (1).

Bit 4/Frame Alignment Signal Bit (1).

Bit 5/Frame Alignment Signal Bit (0).

Bit 6/Frame Alignment Signal Bit (0).

Bit 7/International Bit (Si).

Register Name: **RNAF**
Register Description: **Receive Nonalign Frame Register**
Register Address: **C7h**

Bit #	7	6	5	4	3	2	1	0
Name	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	0	0	0	0	0	0	0

Bit 0/Additional Bit 8 (Sa8).

Bit 1/Additional Bit 7 (Sa7).

Bit 2/Additional Bit 6 (Sa6).

Bit 3/Additional Bit 5 (Sa5).

Bit 4/Additional Bit 4 (Sa4).

Bit 5 / Remote Alarm (A).

Bit 6/Frame Nonalignment Signal Bit (1).

Bit 7/International Bit (Si).

Register Name: **TAF**
Register Description: **Transmit Align Frame Register**
Register Address: **D0h**

Bit #	7	6	5	4	3	2	1	0
Name	Si	0	0	1	1	0	1	1
Default	0	0	0	1	1	0	1	1

Bit 0/Frame Alignment Signal Bit (1).

Bit 1/Frame Alignment Signal Bit (1).

Bit 2/Frame Alignment Signal Bit (0).

Bit 3/Frame Alignment Signal Bit (1).

Bit 4/Frame Alignment Signal Bit (1).

Bit 5/Frame Alignment Signal Bit (0).

Bit 6/Frame Alignment Signal Bit (0).

Bit 7/International Bit (Si).

Register Name: **TNAF**
Register Description: **Transmit Nonalign Frame Register**
Register Address: **D1h**

Bit #	7	6	5	4	3	2	1	0
Name	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	1	0	0	0	0	0	0

Bit 0/Additional Bit 8 (Sa8).

Bit 1/Additional Bit 7 (Sa7).

Bit 2/Additional Bit 6 (Sa6).

Bit 3/Additional Bit 5 (Sa5).

Bit 4/Additional Bit 4 (Sa4).

Bit 5/Remote Alarm (used to transmit the alarm A).

Bit 6/Frame Nonalignment Signal Bit (1).

Bit 7/International Bit (Si).

21.3 Internal Register Scheme Based On CRC4 Multiframe (Method 3)

On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the receive CRC4 multiframe bit in status register 2 (SR4.1). The host can use the SR4.1 bit to know when to read these registers. The user has 2ms to retrieve the data before it is lost. The MSB of each register is the first received. Please see the following register descriptions for more details.

On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that via the transmit Sa bit control register (TSaCR), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the transmit multiframe bit in status register 2 (SR4.4). The host can use the SR4.4 bit to know when to update these registers. It has 2ms to update the data or else the old data will be retransmitted. The MSB of each register is the first bit transmitted. See the following register descriptions for details.

Register Name: **RSiAF**
Register Description: **Receive Si Bits of the Align Frame**
Register Address: **C8h**

Bit #	7	6	5	4	3	2	1	0
Name	SiF0	SiF2	SiF4	SiF6	SiF8	SiF10	SiF12	SiF14
Default	0	0	0	0	0	0	0	0

Bit 0/Si Bit of Frame 14(SiF14).

Bit 1/Si Bit of Frame 12(SiF12).

Bit 2/Si Bit of Frame 10(SiF10).

Bit 3/Si Bit of Frame 8(SiF8).

Bit 4/Si Bit of Frame 6(SiF6).

Bit 5/Si Bit of Frame 4(SiF4).

Bit 6/Si Bit of Frame 2(SiF2).

Bit 7/Si Bit of Frame 0(SiF0).

Register Name: **RSiNAF**
Register Description: **Receive Si Bits of the Nonalign Frame**
Register Address: **C9h**

Bit #	7	6	5	4	3	2	1	0
Name	SiF1	SiF3	SiF5	SiF7	SiF9	SiF11	SiF13	SiF15
Default	0	0	0	0	0	0	0	0

Bit 0/Si Bit of Frame 15(SiF15).

Bit 1/Si Bit of Frame 13(SiF13).

Bit 2/Si Bit of Frame 11(SiF11).

Bit 3/Si Bit of Frame 9(SiF9).

Bit 4/Si Bit of Frame 7(SiF7).

Bit 5/Si Bit of Frame 5(SiF5).

Bit 6/Si Bit of Frame 3(SiF3).

Bit 7/Si Bit of Frame 1(SiF1).

Register Name: **RRA**
Register Description: **Receive Remote Alarm**
Register Address: **CAh**

Bit #	7	6	5	4	3	2	1	0
Name	RRAF1	RRAF3	RRAF5	RRAF7	RRAF9	RRAF11	RRAF13	RRAF15
Default	0	0	0	0	0	0	0	0

Bit 0/Remote Alarm Bit of Frame 15(RRAF15).

Bit 1/Remote Alarm Bit of Frame 13(RRAF13).

Bit 2/Remote Alarm Bit of Frame 11(RRAF11).

Bit 3/Remote Alarm Bit of Frame 9(RRAF9).

Bit 4/Remote Alarm Bit of Frame 7(RRAF7).

Bit 5/Remote Alarm Bit of Frame 5(RRAF5).

Bit 6/Remote Alarm Bit of Frame 3(RRAF3).

Bit 7/Remote Alarm Bit of Frame 1(RRAF1).

Register Name: **RSa4**
Register Description: **Receive Sa4 Bits**
Register Address: **CBh**

Bit #	7	6	5	4	3	2	1	0
Name	RSa4F1	RSa4F3	RSa4F5	RSa4F7	RSa4F9	RSa4F11	RSa4F13	RSa4F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa4 Bit of Frame 15(RSa4F15).

Bit 1/Sa4 Bit of Frame 13(RSa4F13).

Bit 2/Sa4 Bit of Frame 11(RSa4F11).

Bit 3/Sa4 Bit of Frame 9(RSa4F9).

Bit 4/Sa4 Bit of Frame 7(RSa4F7).

Bit 5/Sa4 Bit of Frame 5(RSa4F5).

Bit 6/Sa4 Bit of Frame 3(RSa4F3).

Bit 7/Sa4 Bit of Frame 1(RSa4F1).

Register Name: **RSa5**
Register Description: **Receive Sa5 Bits**
Register Address: **CCh**

Bit #	7	6	5	4	3	2	1	0
Name	RSa5F1	RSa5F3	RSa5F5	RSa5F7	RSa5F9	RSa5F11	RSa5F13	RSa5F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa5 Bit of Frame 15(RSa5F15).

Bit 1/Sa5 Bit of Frame 13(RSa5F13).

Bit 2/Sa5 Bit of Frame 11(RSa5F11).

Bit 3/Sa5 Bit of Frame 9(RSa5F9).

Bit 4/Sa5 Bit of Frame 7(RSa5F7).

Bit 5/Sa5 Bit of Frame 5(RSa5F5).

Bit 6/Sa5 Bit of Frame 3(RSa5F3).

Bit 7/Sa5 Bit of Frame 1(RSa5F1).

Register Name: **RSa6**
Register Description: **Receive Sa6 Bits**
Register Address: **CDh**

Bit #	7	6	5	4	3	2	1	0
Name	RSa6F1	RSa6F3	RSa6F5	RSa6F7	RSa6F9	RSa6F11	RSa6F13	RSa6F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa6 Bit of Frame 15(RSa6F15).

Bit 1/Sa6 Bit of Frame 13(RSa6F13).

Bit 2/Sa6 Bit of Frame 11(RSa6F11).

Bit 3/Sa6 Bit of Frame 9(RSa6F9).

Bit 4/Sa6 Bit of Frame 7(RSa6F7).

Bit 5/Sa6 Bit of Frame 5(RSa6F5).

Bit 6/Sa6 Bit of Frame 3(RSa6F3).

Bit 7/Sa6 Bit of Frame 1(RSa6F1).

Register Name: **RSa7**
Register Description: **Receive Sa7 Bits**
Register Address: **CEh**

Bit #	7	6	5	4	3	2	1	0
Name	RSa7F1	RSa7F3	RSa7F5	RSa7F7	RSa7F9	RSa7F11	RSa7F13	RSa7F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa7 Bit of Frame 15(RSa7F15).

Bit 1/Sa7 Bit of Frame 13(RSa7F13).

Bit 2/Sa7 Bit of Frame 11(RSa7F11).

Bit 3/Sa7 Bit of Frame 9(RSa7F9).

Bit 4/Sa7 Bit of Frame 7(RSa7F7).

Bit 5/Sa7 Bit of Frame 5(RSa7F5).

Bit 6/Sa7 Bit of Frame 3(RSa7F3).

Bit 7/Sa7 Bit of Frame 1(RSa4F1).

Register Name: **RSa8**
Register Description: **Receive Sa8 Bits**
Register Address: **CFh**

Bit #	7	6	5	4	3	2	1	0
Name	RSa8F1	RSa8F3	RSa8F5	RSa8F7	RSa8F9	RSa8F11	RSa8F13	RSa8F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa8 Bit of Frame 15(RSa8F15).

Bit 1/Sa8 Bit of Frame 13(RSa8F13).

Bit 2/Sa8 Bit of Frame 11(RSa8F11).

Bit 3/Sa8 Bit of Frame 9(RSa8F9).

Bit 4/Sa8 Bit of Frame 7(RSa8F7).

Bit 5/Sa8 Bit of Frame 5(RSa8F5).

Bit 6/Sa8 Bit of Frame 3(RSa8F3).

Bit 7/Sa8 Bit of Frame 1(RSa8F1).

Register Name: **TSiAF**
Register Description: **Transmit Si Bits of the Align Frame**
Register Address: **D2h**

Bit #	7	6	5	4	3	2	1	0
Name	TsiF0	TsiF2	TsiF4	TsiF6	TsiF8	TsiF10	TsiF12	TsiF14
Default	0	0	0	0	0	0	0	0

Bit 0/Si Bit of Frame 14(TsiF14).

Bit 1/Si Bit of Frame 12(TsiF12).

Bit 2/Si Bit of Frame 10(TsiF10).

Bit 3/Si Bit of Frame 8(TsiF8).

Bit 4/Si Bit of Frame 6(TsiF6).

Bit 5/Si Bit of Frame 4(TsiF4).

Bit 6/Si Bit of Frame 2(TsiF2).

Bit 7/Si Bit of Frame 0(TsiF0).

Register Name: **TSiNAF**
Register Description: **Transmit Si Bits of the Nonalign Frame**
Register Address: **D3h**

Bit #	7	6	5	4	3	2	1	0
Name	TsiF1	TsiF3	TsiF5	TsiF7	TsiF9	TsiF11	TsiF13	TSiF15
Default	0	0	0	0	0	0	0	0

Bit 0/Si Bit of Frame 15(TSiF15).

Bit 1/Si Bit of Frame 13(TsiF13).

Bit 2/Si Bit of Frame 11(TsiF11).

Bit 3/Si Bit of Frame 9(TsiF9).

Bit 4/Si Bit of Frame 7(TsiF7).

Bit 5/Si Bit of Frame 5(TsiF5).

Bit 6/Si Bit of Frame 3(TsiF3).

Bit 7/Si Bit of Frame 1(TsiF1).

Register Name: **TRA**
Register Description: **Transmit Remote Alarm**
Register Address: **D4h**

Bit #	7	6	5	4	3	2	1	0
Name	TRAF1	TRAF3	TRAF5	TRAF7	TRAF9	TRAF11	TRAF13	TRAF15
Default	0	0	0	0	0	0	0	0

Bit 0/Remote Alarm Bit of Frame 15(TRAF15).

Bit 1/Remote Alarm Bit of Frame 13(TRAF13).

Bit 2/Remote Alarm Bit of Frame 11(TRAF11).

Bit 3/Remote Alarm Bit of Frame 9(TRAF9).

Bit 4/Remote Alarm Bit of Frame 7(TRAF7).

Bit 5/Remote Alarm Bit of Frame 5(TRAF5).

Bit 6/Remote Alarm Bit of Frame 3(TRAF3).

Bit 7/Remote Alarm Bit of Frame 1(TRAF1).

Register Name: **TSa4**
Register Description: **Transmit Sa4 Bits**
Register Address: **D5h**

Bit #	7	6	5	4	3	2	1	0
Name	TSa4F1	TSa4F3	TSa4F5	TSa4F7	TSa4F9	TSa4F11	TSa4F13	TSa4F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa4 Bit of Frame 15(TSa4F15).

Bit 1/Sa4 Bit of Frame 13(TSa4F13).

Bit 2/Sa4 Bit of Frame 11(TSa4F11).

Bit 3/Sa4 Bit of Frame 9(TSa4F9).

Bit 4/Sa4 Bit of Frame 7(TSa4F7).

Bit 5/Sa4 Bit of Frame 5(TSa4F5).

Bit 6/Sa4 Bit of Frame 3(TSa4F3).

Bit 7/Sa4 Bit of Frame 1(TSa4F1).

Register Name: **TSa5**
Register Description: **Transmit Sa5 Bits**
Register Address: **D6h**

Bit #	7	6	5	4	3	2	1	0
Name	TSa5F1	TSa5F3	TSa5F5	TSa5F7	TSa5F9	TSa5F11	TSa5F13	TSa5F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa5 Bit of Frame 15(TSa5F15).

Bit 1/Sa5 Bit of Frame 13(TSa5F13).

Bit 2/Sa5 Bit of Frame 11(TSa5F11).

Bit 3/Sa5 Bit of Frame 9(TSa5F9).

Bit 4/Sa5 Bit of Frame 7(TSa5F7).

Bit 5/Sa5 Bit of Frame 5(TSa5F5).

Bit 6/Sa5 Bit of Frame 3(TSa5F3).

Bit 7/Sa5 Bit of Frame 1(TSa5F1).

Register Name: **TSa6**
Register Description: **Transmit Sa6 Bits**
Register Address: **D7h**

Bit #	7	6	5	4	3	2	1	0
Name	TSa6F1	TSa6F3	TSa6F5	TSa6F7	TSa6F9	TSa6F11	TSa6F13	TSa6F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa6 Bit of Frame 15(TSa6F15).

Bit 1/Sa6 Bit of Frame 13(TSa6F13).

Bit 2/Sa6 Bit of Frame 11(TSa6F11).

Bit 3/Sa6 Bit of Frame 9(TSa6F9).

Bit 4/Sa6 Bit of Frame 7(TSa6F7).

Bit 5/Sa6 Bit of Frame 5(TSa6F5).

Bit 6/Sa6 Bit of Frame 3(TSa6F3).

Bit 7/Sa6 Bit of Frame 1(TSa6F1).

Register Name: **TSa7**
Register Description: **Transmit Sa7 Bits**
Register Address: **D8h**

Bit #	7	6	5	4	3	2	1	0
Name	TSa7F1	TSa7F3	TSa7F5	TSa7F7	TSa7F9	TSa7F11	TSa7F13	TSa7F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa7 Bit of Frame 15(TSa7F15).

Bit 1/Sa7 Bit of Frame 13(TSa7F13).

Bit 2/Sa7 Bit of Frame 11(TSa7F11).

Bit 3/Sa7 Bit of Frame 9(TSa7F9).

Bit 4/Sa7 Bit of Frame 7(TSa7F7).

Bit 5/Sa7 Bit of Frame 5(TSa7F5).

Bit 6/Sa7 Bit of Frame 3(TSa7F3).

Bit 7/Sa7 Bit of Frame 1(TSa4F1).

Register Name: **TSa8**
Register Description: **Transmit Sa8 Bits**
Register Address: **D9h**

Bit #	7	6	5	4	3	2	1	0
Name	TSa8F1	TSa8F3	TSa8F5	TSa8F7	TSa8F9	TSa8F11	TSa8F13	TSa8F15
Default	0	0	0	0	0	0	0	0

Bit 0/Sa8 Bit of Frame 15(TSa8F15).

Bit 1/Sa8 Bit of Frame 13(TSa8F13).

Bit 2/Sa8 Bit of Frame 11(TSa8F11).

Bit 3/Sa8 Bit of Frame 9(TSa8F9).

Bit 4/Sa8 Bit of Frame 7(TSa8F7).

Bit 5/Sa8 Bit of Frame 5(TSa8F5).

Bit 6/Sa8 Bit of Frame 3(TSa8F3).

Bit 7/Sa8 Bit of Frame 1(TSa8F1).

Register Name: **TSACR**
Register Description: **Transmit Sa Bit Control Register**
Register Address: **DAh**

Bit #	7	6	5	4	3	2	1	0
Name	SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	0	0	0	0	0	0	0

Bit 0/Additional Bit 8 Insertion Control Bit (Sa8).
0 = do not insert data from the TSa8 register into the transmit data stream
1 = insert data from the TSa8 register into the transmit data stream

Bit 1/Additional Bit 7 Insertion Control Bit (Sa7).
0 = do not insert data from the TSa7 register into the transmit data stream
1 = insert data from the TSa7 register into the transmit data stream

Bit 2/Additional Bit 6 Insertion Control Bit (Sa6).
0 = do not insert data from the TSa6 register into the transmit data stream
1 = insert data from the TSa6 register into the transmit data stream

Bit 3/Additional Bit 5 Insertion Control Bit (Sa5).
0 = do not insert data from the TSa5 register into the transmit data stream
1 = insert data from the TSa5 register into the transmit data stream

Bit 4/Additional Bit 4 Insertion Control Bit (Sa4).
0 = do not insert data from the TSa4 register into the transmit data stream
1 = insert data from the TSa4 register into the transmit data stream

Bit 5/Remote Alarm Insertion Control Bit (RA).
0 = do not insert data from the TRA register into the transmit data stream
1 = insert data from the TRA register into the transmit data stream

Bit 6/International Bit in Nonalign Frame Insertion Control Bit (SiNAF).
0 = do not insert data from the TSiNAF register into the transmit data stream
1 = insert data from the TSiNAF register into the transmit data stream

Bit 7/International Bit in Align Frame Insertion Control Bit (SiAF).
0 = do not insert data from the TSiAF register into the transmit data stream
1 = insert data from the TSiAF register into the transmit data stream

22. HDLC CONTROLLERS

This device has two enhanced HDLC controllers, HDLC #1 and HDLC #2. Each controller is configurable for use with time slots, or Sa4 to Sa8 bits (E1 Mode) or the FDL (T1 Mode). Each HDLC controller has 128 byte buffers in both the transmit and receive paths. When used with time slots, the user can select any time slot or multiple time slots, contiguous or noncontiguous, as well as any specific bits within the time slot(s) to assign to the HDLC controllers.

The user must take care to not map both transmit HDLC controllers to the same Sa bits, time slots or, in T1 mode, map both controllers to the FDL. HDLC #1 and HDLC #2 are identical in operation and therefore the following operational description refers only to a singular controller.

The HDLC controller performs all the necessary overhead for generating and receiving Performance Report Messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and de-stuffs zeros, and byte aligns to the data stream. The 128-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention.

22.1 Basic Operation Details

To allow the framer to properly source/receive data from/to the HDLC controllers, the legacy FDL circuitry (See the *Legacy FDL Support (T1 Mode)* section.) should be disabled.

The HDLC registers are divided into four groups: control/configuration, status/information, mapping, and FIFOs. Table 24-1 lists these registers by group.

HDLC CONTROLLER REGISTERS Table 24-1

NAME	FUNCTION
CONTROL/CONFIGURATION	
H1TC, HDLC #1 Transmit Control Register **H2TC**, HDLC #2 Transmit Control Register	General control over the transmit HDLC controllers
H1RC, HDLC #1 Receive Control Register **H2RC**, HDLC #2 Receive Control Register	General control over the receive HDLC controllers
H1FC, HDLC #1 FIFO Control Register **H2FC**, HDLC #2 FIFO Control Register	Sets high watermark for receiver and low watermark for transmitter
STATUS/INFORMATION	
SR6, HDLC #1 Status Register **SR7**, HDLC #2 Status Register	Key status information for both transmit and receive directions
IMR6, HDLC #1 Interrupt Mask Register **IMR7**, HDLC #2 Interrupt Mask Register	Selects which bits in Status Registers (SR7 and SR8) will cause interrupts
INFO4, HDLC #1 & #2 Information Register **INFO5**, HDLC #1 Information Register **INFO6**, HDLC #2 Information Register	Information on HDLC controller
H1RPBA, HDLC #1 Receive Packet Bytes Available Register **H2RPBA**, HDLC #2 Receive Packet Bytes Available Register	Indicates the number of bytes that can be read from the receive FIFO
H1TFBA, HDLC #1 Transmit FIFO Buffer Available Register **H2TFBA**, HDLC #2 Transmit FIFO Buffer Available Register	Indicates the number of bytes that can be written to the transmit FIFO
MAPPING	
H1RCS1, H1RCS2, H1RCS3, H1RCS4, HDLC #1 Receive Channel Select Registers **H2RCS1, H2RCS2, H2RCS3, H2RCS4,** HDLC #2 Receive Channel Select Registers	Selects which channels will be mapped to the receive HDLC controller
H1RTSBS, HDLC #1 Receive TS/Sa Bit Select Register **H2RTSBS,** HDLC #2 Receive TS/Sa Bit Select Register	Selects which bits in a channel will be used or which Sa bits will be used by the receive HDLC controller
H1TCS1, H1TCS2, H1TCS3, H1TCS4, HDLC #1 Transmit Channel Select Registers **H2TCS1, H2TCS2, H2TCS3, H2TCS4,** HDLC #2 Transmit Channel Select Registers	Selects which channels will be mapped to the transmit HDLC controller
H1TTSBS, HDLC # 1 Transmit TS/Sa Bit Select Register **H2TTSBS, HDLC # 2** Transmit TS/Sa Bit Select Register	Selects which bits in a channel will be used or which Sa bits will be used by the transmit HDLC controller
FIFOs	
H1RF, HDLC #1 Receive FIFO Register **H2RF**, HDLC #2 Receive FIFO Register	Access to 128-byte receive FIFO
H1TF, HDLC #1 Transmit FIFO Register **H2TF**, HDLC #2 Transmit FIFO Register	Access to 128-byte transmit FIFO

22.2 HDLC Configuration

Basic configuration of the HDLC controllers is accomplished via the HxTC and HxRC registers. Operating features such as CRC generation, zero stuffer, transmit and receive HDLC mapping options, and idle flags are selected here. Also, the HDLC controllers are reset via these registers.

Register Name: **H1TC, H2TC**
Register Description: **HDLC #1 Transmit Control, HDLC #2 Transmit Control**
Register Address: **90h, A0h**

Bit #	7	6	5	4	3	2	1	0
Name	NOFS	TEOML	THR	THMS	TFS	TEOM	TZSD	TCRCD
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit CRC Defeat (TCRCD). A 2-byte CRC code is automatically appended to the outbound message. This bit can be used to disable the CRC function.
0 = enable CRC generation (normal operation)
1 = disable CRC generation

Bit 1/Transmit Zero Stuffer Defeat (TZSD). The zero stuffer function automatically inserts a zero in the message field (between the flags) after five consecutive ones to prevent the emulation of a flag or abort sequence by the data pattern. The receiver automatically removes (de-stuffs) any zero after five ones in the message field.
0 = enable the zero stuffer (normal operation)
1 = disable the zero stuffer

Bit 2/Transmit End of Message (TEOM). Should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO at HxTF. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of the message.

Bit 3/Transmit Flag/Idle Select (TFS). This bit selects the inter-message fill character after the closing and before the opening flags (7Eh).
0 = 7Eh
1 = FFh

Bit 4/Transmit HDLC Mapping Select (THMS).
0 = transmit HDLC assigned to channels
1 = transmit HDLC assigned to FDL (T1 mode), Sa Bits (E1 mode)

Bit 5/Transmit HDLC Reset (THR). Will reset the transmit HDLC controller and flush the transmit FIFO. An abort followed by 7Eh or FFh flags/idle will be transmitted until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent reset.
0 = normal operation
1 = reset transmit HDLC controller and flush the transmit FIFO

Bit 6/Transmit End of Message and Loop (TEOML). To loop on a message, should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO. The message will repeat until the user clears this bit or a new message is written to the transmit FIFO. If the host clears the bit, the looping message will complete then flags will be transmitted until new message is written to the FIFO. If the host terminates the loop by writing a new message to the FIFO the loop will terminate, one or two flags will be transmitted and the new message will start. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of all messages. This is useful for transmitting consecutive SS7 FISUs without host intervention.

Bit 7/Number Of Flags Select (NOFS).
0 = send one flag between consecutive messages
1 = send two flags between consecutive messages

Register Name: **H1RC, H2RC**
Register Description: **HDLC #1 Receive Control, HDLC #2 Receive Control**
Register Address: **31h, 32h**

Bit #	7	6	5	4	3	2	1	0
Name	RHR	RHMS	-	-	-	-	-	RSFD
Default	0	0	0	0	0	0	0	0

Bit 0/Receive SS7 Fill In Signal Unit Delete (RSFD).
0 = normal operation. All FISUs are stored in the receive FIFO and reported to the host.
1 = When a consecutive FISU having the same BSN the previous FISU is detected, it is deleted without host intervention.

Bit 1/Unused, must be set to zero for proper operation.

Bit 2/Unused, must be set to zero for proper operation.

Bit 3/Unused, must be set to zero for proper operation.

Bit 4/Unused, must be set to zero for proper operation.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Receive HDLC Mapping Select (RHMS).
0 = receive HDLC assigned to channels
1 = receive HDLC assigned to FDL (T1 mode), Sa Bits (E1 mode)

Bit 7/Receive HDLC Reset (RHR). Will reset the receive HDLC controller and flush the receive FIFO. Must be cleared and set again for a subsequent reset.
0 = normal operation
1 = reset receive HDLC controller and flush the receive FIFO

22.2.1 FIFO Control

Control of the transmit and receive FIFOs is accomplished via the FIFO control (HxFC). The FIFO control register sets the watermarks for both the transmit and receive FIFO. Bits 3–5 set the transmit low watermark and the lower 3 bits set the receive high watermark.

When the transmit FIFO empties below the low watermark, the TLWM bit in the appropriate HDLC status register SR6 or SR7 will be set. TLWM is a real-time bit and will remain set as long as the transmit FIFO's read pointer is below the watermark. If enabled, this condition can also cause an interrupt via the *INT pin.

When the receive FIFO fills above the high watermark, the RHWM bit in the appropriate HDLC status register will be set. RHWM is a real-time bit and will remain set as long as the receive FIFO's write pointer is above the watermark. If enabled, this condition can also cause an interrupt via the *INT pin.

Register Name: **H1FC, H2FC**
Register Description: **HDLC # 1 FIFO Control, HDLC # 2 FIFO Control**
Register Address: **91h, A1h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	TFLWM2	TFLWM1	TFLWM0	RFHWM2	RFHWM1	RFHWM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2/Receive FIFO High Watermark Select (RFHWM0 to RFHWM2).

RFHWM2	RFHWM1	RFHWM0	RECEIVE FIFO WATERMARK (BYTES)
0	0	0	4
0	0	1	16
0	1	0	32
0	1	1	48
1	0	0	64
1	0	1	80
1	1	0	96
1	1	1	112

Bits 3 to 5/Transmit FIFO Low Watermark Select (TFLWM0 to TFLWM2).

TFLWM2	TFLWM1	TFLWM0	TRANSMIT FIFO WATERMARK (BYTES)
0	0	0	4
0	0	1	16
0	1	0	32
0	1	1	48
1	0	0	64
1	0	1	80
1	1	0	96
1	1	1	112

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

22.3 HDLC Mapping

22.3.1 Receive

The HDLC controllers need to be assigned a space in the T1/E1 bandwidth in which they will transmit and receive data. The controllers can be mapped to either the FDL (T1), Sa bits (E1), or to channels. If mapped to channels, then any channel or combination of channels, contiguous or not, can be assigned to an HDLC controller. When assigned to a channel(s) any combination of bits within the channel(s) can be avoided.

The HxRCS1–HxRCS4 registers are used to assign the receive controllers to channels 1–24 (T1) or 1–32 (E1) according to the following table.

REGISTER	CHANNELS
HxRCS1	1–8
HxRCS2	9–16
HxRCS3	17–24
HxRCS4	25–32

Register Name: **H1RCS1, H1RCS2, H1RCS3, H1RCS4**
H2RCS1, H2RCS2, H2RCS3, H2RCS4
Register Description: **HDLC # 1 Receive Channel Select x**
HDLC # 2 Receive Channel Select x
Register Address: **92h, 93h, 94h, 95h**
A2h, A3h, A4h, A5h

Bit #	7	6	5	4	3	2	1	0
Name	RHCS7	RHCS6	RHCS5	RHCS4	RHCS3	RHCS2	RHCS1	RHCS0
Default	0	0	0	0	0	0	0	0

Bit 0/Receive HDLC Channel Select Bit 0 (RHCS0). Select Channel 1, 9, 17, or 25.

Bit 1/Receive HDLC Channel Select Bit 1 (RHCS1). Select Channel 2, 10, 18, or 26.

Bit 2/Receive HDLC Channel Select Bit 2 (RHCS2). Select Channel 3, 11, 19, or 27.

Bit 3/Receive HDLC Channel Select Bit 3 (RHCS3). Select Channel 4, 12, 20, or 28.

Bit 4/Receive HDLC Channel Select Bit 4 (RHCS4). Select Channel 5, 13, 21, or 29.

Bit 5/Receive HDLC Channel Select Bit 5 (RHCS5). Select Channel 6, 14, 22, or 30.

Bit 6/Receive HDLC Channel Select Bit 6 (RHCS6). Select Channel 7, 15, 23, or 31.

Bit 7/Receive HDLC Channel Select Bit 7 (RHCS7). Select Channel 8, 16, 24, or 32.

Register Name: **H1RTSBS, H2RTSBS**
Register Description: **HDLC # 1 Receive Time Slot Bits/Sa Bits Select**
HDLC # 2 Receive Time Slot Bits/Sa Bits Select
Register Address: **96h, A6h**

Bit #	7	6	5	4	3	2	1	0
Name	RCB8SE	RCB7SE	RCB6SE	RCB5SE	RCB4SE	RCB3SE	RCB2SE	RCB1SE
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Channel Bit 1 Suppress Enable/Sa8 Bit Enable (RCB1SE). LSB of the channel. Set to one to stop this bit from being used when the HDLC is mapped to time slots. Set to one to enable the use of Sa8 bit when HDLC mapped is Sa bits.

Bit 1/Receive Channel Bit 2 Suppress Enable/Sa7 Bit Enable (RCB2SE). Set to one to stop this bit from being used when the HDLC is mapped to time slots. Set to one to enable the use of Sa8 bit when HDLC mapped is Sa bits.

Bit 2/Receive Channel Bit 3 Suppress Enable/Sa6 Bit Enable (RCB3SE). Set to one to stop this bit from being used when the HDLC is mapped to time slots. Set to one to enable the use of Sa8 bit when HDLC mapped is Sa bits.

Bit 3/Receive Channel Bit 4 Suppress Enable/Sa5 Bit Enable (RCB4SE). Set to one to stop this bit from being used when the HDLC is mapped to time slots. Set to one to enable the use of Sa8 bit when HDLC mapped is Sa bits.

Bit 4/Receive Channel Bit 5 Suppress Enable/Sa4 Bit Enable (RCB5SE). Set to one to stop this bit from being used when the HDLC is mapped to time slots. Set to one to enable the use of Sa8 bit when HDLC mapped is Sa bits.

Bit 5/Receive Channel Bit 6 Suppress Enable (RCB6SE). Set to one to stop this bit from being used.

Bit 6/Receive Channel Bit 7 Suppress Enable (RCB7SE). Set to one to stop this bit from being used.

Bit 7/Receive Channel Bit 8 Suppress Enable (RCB8SE). MSB of the channel. Set to one to stop this bit from being used.

22.3.2 Transmit

The HxTCS1–HxTCS4 registers are used to assign the transmit controllers to channels 1–24 (T1) or 1–32 (E1), according to the following table.

REGISTER	CHANNELS
HxTCS1	1–8
HxTCS2	9–16
HxTCS3	17–24
HxTCS4	25–32

Register Name: **H1TCS1, H1TCS2, H1TCS3, H1TCS4**
H2TCS1, H2TCS2, H2TCS3, H2TCS4

Register Description: **HDLC # 1 Transmit Channel Select**
HDLC # 2 Transmit Channel Select

Register Address: **97h, 98h, 99h, 9Ah**
A7h, A8h, A9h, AAh

Bit #	7	6	5	4	3	2	1	0
Name	THCS7	THCS6	THCS5	THCS4	THCS3	THCS2	THCS1	THCS0
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit HDLC Channel Select Bit 0 (THCS0). Select Channel 1, 9, 17, or 25.

Bit 1/Transmit HDLC Channel Select Bit 1 (THCS1). Select Channel 2, 10, 18, or 26.

Bit 2/Transmit HDLC Channel Select Bit 2 (THCS2). Select Channel 3, 11, 19, or 27.

Bit 3/Transmit HDLC Channel Select Bit 3 (THCS3). Select Channel 4, 12, 20, or 28.

Bit 4/Transmit HDLC Channel Select Bit 4 (THCS4). Select Channel 5, 13, 21, or 29.

Bit 5/Transmit HDLC Channel Select Bit 5 (THCS5). Select Channel 6, 14, 22, or 30.

Bit 6/Transmit HDLC Channel Select Bit 6 (THCS6). Select Channel 7, 15, 23, or 31.

Bit 7/Transmit HDLC Channel Select Bit 7 (THCS7). Select Channel 8, 16, 24, or 32.

Register Name: **H1TTSBS, H2TTSBS**
Register Description: **HDLC # 1 Transmit Time Slot Bits/Sa Bits Select**
HDLC # 2 Transmit Time Slot Bits/Sa Bits Select
Register Address: **9Bh, Abh**

Bit #	7	6	5	4	3	2	1	0
Name	TCB8SE	TCB7SE	TCB6SE	TCB5SE	TCB4SE	TCB3SE	TCB2SE	TCB1SE
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit Channel Bit 1 Suppress Enable / Sa8 Bit Enable (TCB1SE). LSB of the channel. Set to one to stop this bit from being used.

Bit 1/Transmit Channel Bit 2 Suppress Enable/ Sa7 Bit Enable (TCB1SE). Set to one to stop this bit from being used.

Bit 2/Transmit Channel Bit 3 Suppress Enable/Sa6 Bit Enable (TCB1SE). Set to one to stop this bit from being used.

Bit 3/Transmit Channel Bit 4 Suppress Enable/Sa5 Bit Enable (TCB1SE). Set to one to stop this bit from being used.

Bit 4/Transmit Channel Bit 5 Suppress Enable/Sa4 Bit Enable (TCB1SE). Set to one to stop this bit from being used.

Bit 5/Transmit Channel Bit 6 Suppress Enable (TCB1SE). Set to one to stop this bit from being used.

Bit 6/Transmit Channel Bit 7 Suppress Enable (TCB1SE). Set to one to stop this bit from being used.

Bit 7/Transmit Channel Bit 8 Suppress Enable (TCB1SE). MSB of the channel. Set to one to stop this bit from being used.

Register Name: **SR6, SR7**
Register Description: **HDLC #1 Status Register 6**
HDLC #2 Status Register 7
Register Address: **20h, 22h**

Bit #	7	6	5	4	3	2	1	0
Name	-	TMEND	RPE	RPS	RHWM	RNE	TLWM	TNF
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit FIFO Not Full Condition (TNF). Set when the transmit 128-byte FIFO has at least one byte available.

Bit 1/Transmit FIFO Below Low Watermark Condition (TLWM). Set when the transmit 128-byte FIFO empties beyond the low watermark as defined by the Transmit Low Watermark Register (TLWMR).

Bit 2/Receive FIFO Not Empty Condition (RNE). Set when the receive 128-byte FIFO has at least one byte available for a read.

Bit 3/Receive FIFO Above High Watermark Condition (RHWM). Set when the receive 128-byte FIFO fills beyond the high watermark as defined by the receive high-watermark register (RHWMR).

Bit 4/Receive Packet Start Event (RPS). Set when the HDLC controller detects an opening byte. This is a latched bit and will be cleared when read.

Bit 5/Receive Packet End Event (RPE). Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. This is a latched bit and will be cleared when read.

Bit 6/Transmit Message End Event (TMEND). Set when the transmit HDLC controller has finished sending a message. This is a latched bit and will be cleared when read.

Register Name: **IMR6, IMR7**
Register Description: **HDLC # 1 Interrupt Mask Register 6**
HDLC # 2 Interrupt Mask Register 7
Register Address: **21h, 23h**

Bit #	7	6	5	4	3	2	1	0
Name	-	TMEND	RPE	RPS	RHWM	RNE	TLWM	TNF
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit FIFO Not Full Condition (TNF).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 1/Transmit FIFO Below Low Watermark Condition (TLWM).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 2/Receive FIFO Not Empty Condition (RNE).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 3/Receive FIFO Above High Watermark Condition (RHWM).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising edge only

Bit 4/Receive Packet Start Event (RPS).
0 = interrupt masked
1 = interrupt enabled

Bit 5/Receive Packet End Event (RPE).
0 = interrupt masked
1 = interrupt enabled

Bit 6/Transmit Message End Event (TMEND).
0 = interrupt masked
1 = interrupt enabled

Register Name: **INFO5, INFO6**
Register Description: **HDLC #1 Information Register**
HDLC #2 Information Register
Register Address: **2Eh, 2Fh**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	TEMPTY	TFULL	REMPTY	PS2	PS1	PS0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2/Receive Packet Status (PS0 to PS2). These are real-time bits indicating the status as of the last read of the receive FIFO.

PS2	PS1	PS0	PACKET STATUS
0	0	0	**In Progress:** End of message has not yet been reached
0	0	1	**Packet OK:** Packet ended with correct CRC code word
0	1	0	**CRC Error:** A closing flag was detected, preceded by a corrupt CRC code word
0	1	1	**Abort:** Packet ended because an abort signal was detected (seven or more ones in a row)
1	0	0	**Overrun:** HDLC controller terminated reception of packet because receive FIFO is full
1	0	1	**Message Too Short:** Three or fewer bytes including CRC

Bit 3/Receive FIFO Empty (REMPTY). A real-time bit that is set high when the receive FIFO is empty.

Bit 4/Transmit FIFO Full (TFULL). A real-time bit that is set high when the FIFO is full.

Bit 5/Transmit FIFO Empty (TEMPTY). A real-time bit that is set high when the FIFO is empty.

Register Name: **INFO4**
Register Description: **HDLC Event Information Register #4**
Register Address: **2Dh**

Bit #	7	6	5	4	3	2	1	0
Name					H2UDR	H2OBT	H1UDR	H1OBT
Default	0	0	0	0	0	0	0	0

Bit 0/HDLC #1 Opening Byte Event (H1OBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Bit 1/HDLC #1 Transmit FIFO Underrun Event (H1UDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent. This bit is latched and will be cleared when read.

Bit 2/HDLC #2 Opening Byte Event (H2OBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Bit 3/HDLC #2 Transmit FIFO Underrun Event (H2UDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent. This bit is latched and will be cleared when read.

22.3.3 FIFO Information

The transmit FIFO buffer-available register indicates the number of bytes that can be written into the transmit FIFO. The count from this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer.

Register Name: **H1TFBA, H2TFBA**
Register Description: **HDLC # 1 Transmit FIFO Buffer Available**
HDLC # 2 Transmit FIFO Buffer Available
Register Address: **9Fh, Afh**

Bit #	7	6	5	4	3	2	1	0
Name	TFBA7	TFBA6	TFBA5	TFBA4	TFBA3	TFBA2	TFBA1	TFBA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Transmit FIFO Bytes Available (TFBAO to TFBA7). TFBA0 is the LSB.

22.3.4 Receive Packet Bytes Available

The lower 7 bits of the receive packet bytes available register indicate the number of bytes (0 through 127) that can be read from the receive FIFO. The value indicated by this register (lower 7 bits) informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value will refer to one of four possibilities: the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register, the host then checks the HDLC information register for detailed message status.

If the value in the HxRPBA register refers to the beginning portion of a message or continuation of a message then the MSB of the HxRPBA register will return a value of 1. This indicates that the host can safely read the number of bytes returned by the lower 7 bits of the HxRPBA register but there is no need to check the information register since the packet has not yet terminated (successfully or otherwise).

Register Name: **H1RPBA, H2RPBA**
Register Description: **HDLC # 1 Receive Packet Bytes Available**
HDLC # 2 Receive Packet Bytes Available
Register Address: **9Ch, Ach**

Bit #	7	6	5	4	3	2	1	0
Name	MS	RPBA6	RPBA5	RPBA4	RPBA3	RPBA2	RPBA1	RPBA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 6/Receive FIFO Packet Bytes Available Count (RPBA0 to RPBA6). RPBA0 is the LSB.

Bit 7/Message Status (MS).
0 = bytes indicated by RPBA0 through RPBA6 are the end of a message. Host must check the INFO5 or INFO6 register for details.
1 = bytes indicated by RPBA0 through RPBA6 are the beginning or continuation of a message. The host does not need to check the INFO5 or INFO6 register.

22.3.5 HDLC FIFOS

Register Name: **H1TF, H2TF**
Register Description: **HDLC # 1 Transmit FIFO, HDLC # 2 Transmit FIFO**
Register Address: **9Dh, Adh**

Bit #	7	6	5	4	3	2	1	0
Name	THD7	THD6	THD5	THD4	THD3	THD2	THD1	THD0
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit HDLC Data Bit 0 (THD0). LSB of a HDLC packet data byte.

Bit 1/Transmit HDLC Data Bit 1 (THD1).

Bit 2/Transmit HDLC Data Bit 2 (THD2).

Bit 3/Transmit HDLC Data Bit 3 (THD3).

Bit 4/Transmit HDLC Data Bit 4 (THD4).

Bit 5/Transmit HDLC Data Bit 5 (THD5).

Bit 6/Transmit HDLC Data Bit 6 (THD6).

Bit 7/Transmit HDLC Data Bit 7 (THD7). MSB of a HDLC packet data byte.

Register Name: **H1RF, H2RF**
Register Description: **HDLC # 1 Receive FIFO, HDLC # 2 Receive FIFO**
Register Address: **9Eh, Aeh**

Bit #	7	6	5	4	3	2	1	0
Name	RHD7	RHD6	RHD5	RHD4	RHD3	RHD2	RHD1	RHD0
Default	0	0	0	0	0	0	0	0

Bit 0/Receive HDLC Data Bit 0 (RHD0). LSB of a HDLC packet data byte.

Bit 1/Receive HDLC Data Bit 1 (RHD1).

Bit 2/Receive HDLC Data Bit 2 (RHD2).

Bit 3/Receive HDLC Data Bit 3 (RHD3).

Bit 4/Receive HDLC Data Bit 4 (RHD4).

Bit 5/Receive HDLC Data Bit 5 (RHD5).

Bit 6/Receive HDLC Data Bit 6 (RHD6).

Bit 7/Receive HDLC Data Bit 7 (RHD7). MSB of a HDLC packet data byte.

22.4 Receive HDLC Code Example

Below is an example of a receive HDLC routine for controller #1.

1) Reset receive HDLC controller
2) Set HDLC mode, mapping, and high watermark
3) Start new message buffer
4) Enable RPE and RHWM interrupts
5) Wait for interrupt
6) Disable RPE and RHWM interrupts
7) Read HxRPBA register. N = HxRPBA (lower 7 bits are byte count, MSB is status)
8) Read (N AND 7Fh) bytes from receive FIFO and store in message buffer
9) Read INFO5 register
10) If PS2, PS1, PS0 = 000, then go to step 4
11) If PS2, PS1, PS0 = 001, then packet terminated OK, save present message buffer
12) If PS2, PS1, PS0 = 010, then packet terminated with CRC error
13) If PS2, PS1, PS0 = 011, then packet aborted
14) If PS2, PS1, PS0 = 100, then FIFO overflowed
15) Go to step 3

22.5 Legacy FDL Support (T1 Mode)

In order to provide backward compatibility to the older DS21x52 T1 device, the DS21Q55 maintains the circuitry that existed in the previous generation of the T1 framer. In new applications, it is recommended that the HDLC controllers and BOC controller are used.

22.5.1 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2ms (8 x 250µs). The framer will signal an external microcontroller that the buffer has filled via the SR8.3 bit. If enabled via IMR8.3, the INT pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR8.1 bit will be set to a one and the INT pin will toggled low if enabled via IMR8.1. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The framer also contains a zero destuffer, which is controlled via the T1RCR2.3 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via T1RCR2.3, the device will automatically look for five ones in a row, followed by a zero. If it finds such a pattern, it will automatically remove the zero. If the zero destuffer sees six or more ones in a row followed by a zero, the zero is not removed. The T1RCR2.3 bit should always be set to a one when the device is extracting the FDL. More on how to use the DS21Q55 in FDL applications in this legacy support mode is covered in a separate application note.

Register Name: **RFDL**
Register Description: **Receive FDL Register**
Register Address: **C0h**

Bit #	7	6	5	4	3	2	1	0
Name	RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0
Default	0	0	0	0	0	0	0	0

Bit 0/Receive FDL Bit 0 (RFDL0). LSB of the Received FDL Code.

Bit 1/Receive FDL Bit 1 (RFDL1).

Bit 2/Receive FDL Bit 2 (RFDL2).

Bit 3/Receive FDL Bit 3 (RFDL3).

Bit 4/Receive FDL Bit 4 (RFDL4).

Bit 5/Receive FDL Bit 5 (RFDL5).

Bit 6/Receive FDL Bit 6 (RFDL6).

Bit 7/Receive FDL Bit 7 (RFDL7). MSB of the Received FDL Code.

The receive FDL register (RFDL) reports the incoming facility data link (FDL) or the incoming Fs bits. The LSB is received first.

Register Name: **RFDLM1, RFDLM2**
Register Description: **Receive FDL Match Register 1**
Receive FDL Match Register 2
Register Address: **C2h, C3h**

Bit #	7	6	5	4	3	2	1	0
Name	RFDLM7	RFDLM6	RFDLM5	RFDLM4	RFDLM3	RFDLM2	RFDLM1	RFDLM0
Default	0	0	0	0	0	0	0	0

Bit 0/Receive FDL Match Bit 0 (RFDLM0). LSB of the FDL Match Code.

Bit 1/Receive FDL Match Bit 1 (RFDLM1).

Bit 2/Receive FDL Match Bit 2 (RFDLM2).

Bit 3/Receive FDL Match Bit 3 (RFDLM3).

Bit 4/Receive FDL Match Bit 4 (RFDLM4).

Bit 5/Receive FDL Match Bit 5 (RFDLM5).

Bit 6/Receive FDL Match Bit 6 (RFDLM6).

Bit 7/Receive FDL Match Bit 7 (RFDLM7). MSB of the FDL Match Code.

22.5.2 Transmit Section

The transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full eight bits has been shifted out, the framer will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR8.2 bit to a one. The INT will also toggle low if enabled via IMR8.2. The user has 2ms to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again. The framer also contains a zero stuffer which is controlled via the T1TCR2.5 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via T1TCR2.5, the framer will automatically look for 5 ones in a row. If it finds such a pattern, it will automatically insert a zero after the five ones. The T1TCR2.5 bit should always be set to a one when the framer is inserting the FDL.

Register Name: **TFDL**
Register Description: **Transmit FDL Register**
Register Address: **C1h**

Bit #	7	6	5	4	3	2	1	0
Name	TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0
Default	0	0	0	0	0	0	0	0

(Note: Also used to insert Fs framing pattern in D4 framing mode)

Bit 0/Transmit FDL Bit 0 (TFDL0). LSB of the Transmit FDL Code.

Bit 1/Transmit FDL Bit 1 (TFDL1).

Bit 2/Transmit FDL Bit 2 (TFDL2).

Bit 3/Transmit FDL Bit 3 (TFDL3).

Bit 4/Transmit FDL Bit 4 (TFDL4).

Bit 5/Transmit FDL Bit 5 (TFDL5).

Bit 6/Transmit FDL Bit 6 (TFDL6).

Bit 7/Transmit FDL Bit 7 (TFDL7). MSB of the Transmit FDL Code.

The transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first.

22.6 D4/SLC–96 Operation

In the D4 framing mode, the framer uses the TFDL register to insert the Fs framing pattern. To allow the device to properly insert the Fs framing pattern, the TFDL register at address C1h must be programmed to 1Ch and the following bits must be programmed as shown: T1TCR1.2 = 0 (source Fs data from the TFDL register) T1TCR2.6 = 1 (allow the TFDL register to load on multiframe boundaries).

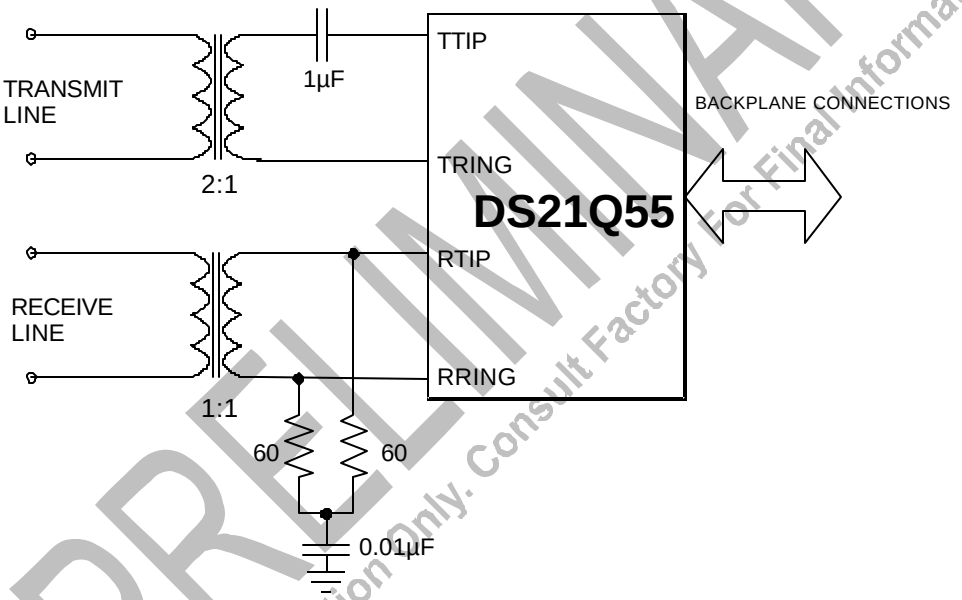
Since the SLC–96 message fields share the Fs-bit position, the user can access these message fields via the TFDL and RFDL registers. Please see the separate application note for a detailed description of how to implement a SLC–96 function.

23. LINE INTERFACE UNIT (LIU)

The LIU in the DS21Q55 contains three sections: the receiver, which handles clock and data recovery; the transmitter, which wave-shapes and drives the network line; and the jitter attenuator. These three sections are controlled by the line interface control registers (LIC1–LIC4), which are described below. The LIU has its own T1/E1 mode select bit and can operate independently of the framer function.

The DS21Q55 can switch between T1 or E1 networks without changing any external components on either the transmit or receive side. Figure 25-1 shows a network connection using minimal components. In this configuration the device can connect to T1, J1, or E1 (75O or 120O) without any component change. The receiver can adjust the 120O termination to 100O or 75O. The transmitter can adjust its output impedance to provide high return loss characteristics for 120O, 100O, and 75O lines. Other components may be added to this configuration in order to meet safety and network protection requirements. This is covered in *Recommended Circuits.*

BASIC NETWORK CONNECTIONS Figure 25-1



23.1 LIU Operation

The analog AMI/HDB3 waveform off of the E1 line or the AMI/B8ZS waveform off of the T1 line is transformer coupled into the RTIP and RRING pins of the DS21Q55. The user has the option to use internal termination, software selectable for 75Ω/100Ω/120Ω applications, or external termination. The LIU recovers clock and data from the analog signal and passes it through the jitter attenuation MUX outputting the received line clock at RCLKO and bipolar or NRZ data at RPOSO and RNEGO. The DS21Q55 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The receive circuitry also is configurable for various monitor applications. The device has a usable receive sensitivity of 0dB to -43dB for E1 and 0dB to -36dB for T1, which allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input at TPOSI and TNEGI is sent via the jitter attenuation MUX to the wave shaping circuitry and line driver. The DS21Q55 will drive the E1 or T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for T1.

23.2 LIU Receiver

The DS21Q55 contains a digital clock recovery system. The device couples to the receive E1 or T1 twisted pair (or coaxial cable in 75Ω E1 applications) via a 1:1 transformer. See Table 25-1 for transformer details. The DS21Q55 has the option of using software-selectable termination requiring only a single, fixed pair of termination resistors.

The DS21Q55's LIU is designed to be fully software selectable for E1 and T1 without the need to change any external resistors for the receive-side. The receive-side will allow the user to configure the device for 75Ω, 100Ω, or 120Ω receive termination by setting the RT1 (LIC4.1) and RT0 (LIC4.0) bits. When using the internal termination feature, the resistors labeled R in Figure should be 60Ω each. If external termination is required, RT1 and RT0 should be set to zero and the resistors labeled R in Figure will need to be 37.5Ω, 50Ω, or 60Ω each depending on the line impedance.

There are two ranges of receive sensitivity for both T1 and E1, which is selectable by the user. The EGL bit of LIC1 (LIC1.4) selects the full or limited sensitivity.

The resultant E1 or T1 clock derived from MCLK is multiplied by 16 via an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times over-sampler, which is used to recover the clock and data. This over-sampling technique offers outstanding performance to meet jitter tolerance specifications shown in.

Normally, the clock that is output at the RCLK pin is the recovered clock from the E1 AMI/HDB3 or T1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit slightly shorter high cycles of the clock. This is due to the highly over-sampled digital clock recovery circuitry. See *Receive AC Timing Characteristics* for more details. When no signal is present at RTIP and RRING, a receive carrier loss (RCL) condition will occur and the RCLK will be derived from the JACLK source.

23.2.1 Receive Level Indicator and Threshold Interrupt

The DS21Q55 reports the signal strength at RTIP and RRING in 2.5dB increments through RL3–RL0 located in Information Register 2 (INFO2). This feature is helpful when trouble-shooting line-performance problems. The DS2155 can initiate an interrupt whenever the input falls below a certain level through the input-level under-threshold indicator (SR1.7). Using the RLT0–RLT4 bits of the CCR4 register, the user can set a threshold in 2.5dB increments. The SR1.7 bit is set whenever the input level at RTIP and RRING falls below the threshold set by the value in RLT0–RLT4. The level must remain below the programmed threshold for approximately 50ms for this bit to be set.

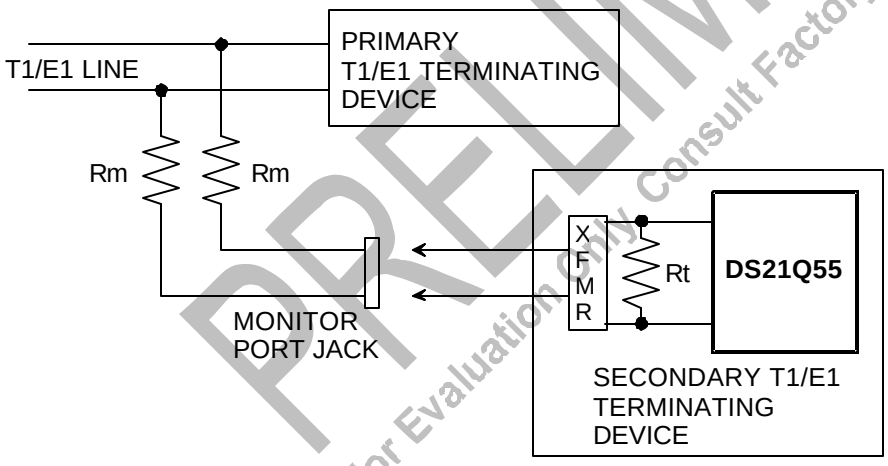
23.2.2 Receive G.703 Synchronization Signal (E1 Mode)

The DS21Q55 is capable of receiving a 2.048MHz square-wave synchronization clock as specified in Section 13 of ITU G.703 10/98. In order to use this mode, set the receive synchronization clock Enable (LIC3.2) = 1.

23.2.3 Monitor Mode

Monitor applications in both E1 and T1 require various flat gain settings for the receive-side circuitry. The DS21Q55 can be programmed to support these applications via the monitor mode control bits MM1 and MM0 in the LIC3 register (Figure 25-2).

TYPICAL MONITOR APPLICATION Figure 25-2



23.3 LIU Transmitter

The DS21Q55 uses a phase-lock loop along with a precision digital-to-analog converter (DAC) to create the waveforms that are transmitted onto the E1 or T1 line. The waveforms created by the transmitter meet the latest ETSI, ITU, ANSI, and AT&T specifications. The user will select which waveform is to be generated by setting the ETS bit (LIC2.7) for E1 or T1 operation, then programming the L2/L1/L0 bits in register LIC1 for the appropriate application.

A 2.048MHz or 1.544MHz clock is required at TCLKI for transmitting data presented at TPOSI and TNEGI. Normally these pins are connected to TCLKO, TPOSO and TNEGO. However, the LIU may operate in an independent fashion. ITU specification G.703 requires an accuracy of ±50ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of ±32ppm for T1 interfaces. The clock can be sourced internally from RCLK or JACLK. See LIC2.3, LIC4.4 and LIC4.5 for details. Due to the nature of the design of the transmitter, very little jitter (less than 0.005 UIpp broadband from 10Hz to 100kHz) is added to the jitter present on TCLK. Also, the waveforms created are independent of the duty cycle of TCLK. The transmitter couples to the E1 or T1 transmit twisted pair (or coaxial cable in some E1 applications) via a 1:2 step-up transformer. In order for the device to create the proper waveforms, the transformer used must meet the specifications listed in Table 25-1. The DS21Q55 has the option of using software-selectable transmit termination.

The transmit line drive has two modes of operation: fixed gain or automatic gain. In the fixed gain mode, the transmitter outputs a fixed current into the network load to achieve a nominal pulse amplitude. In the automatic gain mode, the transmitter adjusts its output level to compensate for slight variances in the network load. See the *Transmit Line Build-Out Control (TLBC)* register for details.

23.3.1 Transmit Short-Circuit Detector/Limiter

The DS21Q55 has automatic short-circuit limiter which limits the source current to 50mA (rms) into a 1 ohm load. This feature can be disabled by setting the SCLD bit (LIC2.1) = 1. TCLE (INFO2.5) provides a real time indication of when the current limiter is activated. If the current limiter is disabled, TCLE will indicate that a short-circuit condition exist. Status Register SR1.2 provides a latched version of the information, which can be used to activate an interrupt when enable via the IMR1 register. When set low, the TPD bit (LIC1.0) will power-down the transmit line driver and tristate the TTIP and TRING pins.

23.3.2 Transmit Open-Circuit Detector

The DS21Q55 can also detect when the TTIP or TRING outputs are open circuited. TOCD (INFO2.4) will provide a real-time indication of when an open circuit is detected. SR1 provides a latched version of the information (SR1.1), which can be used to activate an interrupt when enable via the IMR1 register.

23.3.3 Transmit BPV Error Insertion

When IBPV (LIC2.5) is transitioned from a zero to a one, the device waits for the next occurrence of three consecutive ones to insert a BPV. IBPV must be cleared and set again for another BPV error insertion.

23.3.4 Transmit G.703 Synchronization Signal (E1 Mode)

The DS21Q55 can transmit the 2.048MHz square-wave synchronization clock As defined in section 13 of ITU G.703 10/98. In order to transmit the 2.048MHz clock, when in E1 mode, set the transmit synchronization clock enable (LIC3.1) = 1.

23.4 MCLK Prescaler

A 16.384MHz, 8.192MHz, 4.096MHz, 2.048MHz, or 1.544MHz clock must be applied at MCLK. ITU specification G.703 requires an accuracy of ±50ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of ±32ppm for T1 interfaces. A prescaler will divide the 16MHz, 8MHz, or 4MHz clock down to 2.048MHz. There is an onboard PLL for the jitter attenuator that will convert the 2.048MHz clock to a 1.544MHz rate for T1 applications. Setting JAMUX (LIC2.3) to a logic 0 bypasses this PLL.

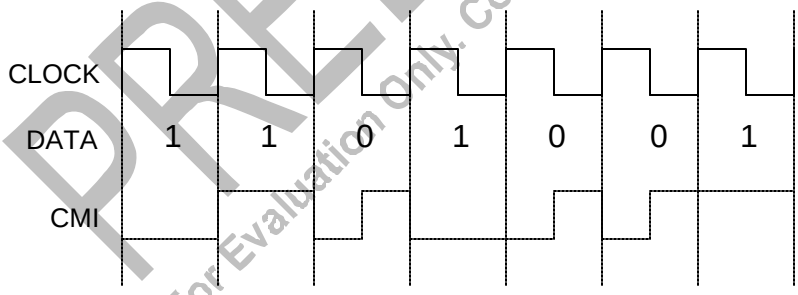
23.5 Jitter Attenuator

The DS21Q55 contains an onboard jitter attenuator that can be set to a depth of either 32 bits or 128 bits via the JABDS bit (LIC1.2). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay-sensitive applications. The characteristics of the attenuation are shown in Figure 14. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit (LIC1.3). Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit (LIC1.1). Onboard circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLK pin to create a smooth jitter free clock which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLK pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either 120UIpp (buffer depth is 128 bits) or 28UIpp (buffer depth is 32 bits), then the jitter attenuator will divide the internal nominal 32.768MHz (E1) or 24.704MHz (T1) clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in Status Register 1 (SR1.4).

23.6 CMI (Code Mark Inversion) Option

The DS21Q55 provides a CMI interface for connection to optical transports. This interface is a unipolar 1T2B type of signal. Ones are encoded as either a logical one or zero level for the full duration of the clock period. Zeros are encoded as a zero-to-one transition at the middle of the clock period.

CMI CODING Figure 25-3



Transmit and receive CMI is enabled via LIC4.7. When this register bit is set, the TTIP pin will output CMI coded data at normal levels. This signal can be used to directly drive an optical interface. When CMI is enable, the user can also use HDB3/B8ZS coding. When this register bit is set, the RTIP pin will become a unipolar CMI input. The CMI signal will be processed to extract and align the clock with data.

23.7 LIU Control Registers

Register Name: **LIC1**
Register Description: **Line Interface Control 1**
Register Address: **78h**

Bit #	7	6	5	4	3	2	1	0
Name	L2	L1	L0	EGL	JAS	JABDS	DJA	TPD
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit Power-Down (TPD).
0 = powers down the transmitter and tristates the TTIP and TRING pins
1 = normal transmitter operation

Bit 1/Disable Jitter Attenuator (DJA).
0 = jitter attenuator enabled
1 = jitter attenuator disabled

Bit 2/Jitter Attenuator Buffer Depth Select (JABDS).
0 = 128 bits
1 = 32 bits (use for delay sensitive applications)

Bit 3/Jitter Attenuator Select (JAS).
0 = place the jitter attenuator on the receive side
1 = place the jitter attenuator on the transmit side

Bit 4/Receive Equalizer Gain Limit (EGL). This bit controls the sensitivity of the receive equalizer.
T1 Mode: 0 = -36dB (long haul)
1 = -15dB (limited long haul)
E1 Mode: 0 = -15dB (short haul)
1 = -43dB (long haul)

Bits 5 to 7/Line Build-Out Select (L0 to L2). When using the internal termination the user needs only to select 000 for 75O operation or 001 for 120O operation below. This selects the proper voltage levels for 75O or 120O operation. Using TT0 and TT1 of the LICR4 register, users can then select the proper internal source termination. Line build-outs 100 and 101 are for backwards compatibility with older products only.

E1 Mode

L2	L1	L0	APPLICATION	N (1)	RETURN LOSS	Rt (1)
0	0	0	75O normal	1:2	NM	0
0	0	1	120O normal	1:2	NM	0
1	0	0	75O with high return loss*	1:2	21dB	6.2O
1	0	1	120O with high return loss*	1:2	21dB	11.6O

*****TT0 and TT1 of LIC4 register must be set to zero in this configuration.

T1 Mode

L2	L1	L0	APPLICATION	N (1)	RETURN LOSS	Rt (1)
0	0	0	DSX-1 (0 to 133 feet)/0dB CSU	1:2	NM	0
0	0	1	DSX-1 (133 to 266 feet)	1:2	NM	0
0	1	0	DSX-1 (266 to 399 feet)	1:2	NM	0
0	1	1	DSX-1 (399 to 533 feet)	1:2	NM	0
1	0	0	DSX-1 (533 to 655 feet)	1:2	NM	0
1	0	1	-7.5dB CSU	1:2	NM	0
1	1	0	-15dB CSU	1:2	NM	0
1	1	1	-22.5dB CSU	1:2	NM	0

Register Name: **TLBC**
Register Description: **Transmit Line Build-Out Control**
Register Address: **7Dh**

Bit #	7	6	5	4	3	2	1	0
Name	-	AGCE	GC5	GC4	GC3	GC2	GC1	GC0
Default	0	0	0	0	0	0	0	0

Bit 0–5 Gain Control Bits 0–5 (GC0–GC5). The GC0 through GC5 bits control the gain setting for the nonautomatic gain mode. Use the tables below for setting the recommended values. The LB (line build-out) column refers to the value in the L0–L2 bits in LIC1 (Line Interface Control 1) register.

NETWORK MODE	LB	GC5	GC4	GC3	GC2	GC1	GC0
T1, Impedance Match Off	0	1	0	0	1	1	0
	1	0	1	1	0	1	1
	2	0	1	1	0	1	0
	3	1	0	0	0	0	0
	4	1	0	0	1	1	1
	5	1	0	0	1	1	1
	6	0	1	0	0	1	1
	7	1	1	1	1	1	1
T1, Impedance Match On	0	0	1	1	1	1	0
	1	0	1	0	1	0	1
	2	0	1	0	1	0	1
	3	0	1	1	0	1	0
	4	1	0	0	0	1	0
	5	1	0	0	0	0	0
	6	0	0	1	1	0	0
	7	1	1	1	1	1	1
E1, Impedance Match Off	0	1	0	0	0	0	1
	1	1	0	0	0	0	1
	4	1	0	1	0	1	0
	5	1	0	1	0	0	0
E1, Impedance Match On	1	0	1	1	0	1	0
	2	0	1	1	0	1	0

Bit 6/Automatic Gain Control Enable (AGCE).
0 = use Transmit AGC, TLBC bits 0–5 are "don't care"
1 = do not use Transmit AGC, TLBC bits 0–5 set nominal level

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **LIC2**
Register Description: **Line Interface Control 2**
Register Address: **79h**

Bit #	7	6	5	4	3	2	1	0
Name	ETS	LIRST	IBPV	TUA1	JAMUX	-	SCLD	CLDS
Default	0	0	0	0	0	0	0	0

Bit 0 Custom Line Driver Select (CLDS). Setting this bit to a one will redefine the operation of the transmit line driver. When this bit is set to a one and LIC1.5 = LIC1.6 = LIC1.7 = 0, then the device will generate a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to a one and LIC1.5 = LIC1.6 = LIC1.7 ≠ 0, then the device will force TTIP and TRING outputs to become open-drain drivers instead of their normal push-pull operation. This bit should be set to zero for normal operation of the device.

Bit 1/Short Circuit Limit Disable (ETS = 1) (SCLD). Controls the 50mA (rms) current limiter.
0 = enable 50mA current limiter
1 = disable 50mA current limiter

Bit 2/Unused, must be set to zero for proper operation.

Bit 3/Jitter Attenuator MUX (JAMUX). Controls the source for JACLK.
0 = JACLK sourced from MCLK (2.048MHz or 1.544MHz at MCLK)
1 = JACLK sourced from internal PLL (2.048MHz at MCLK)

Bit 4/Transmit Unframed All Ones (TUA1). The polarity of this bit is set such that the device will transmit an all ones pattern on power-up or device reset. This bit must be set to a one to allow the device to transmit data. The transmission of this data pattern is always timed off of the JACLK.
0 = transmit all ones at TTIP and TRING
1 = transmit data normally

Bit 5/Insert BPV (IBPV). A zero-to-one transition on this bit will cause a single BPV to be inserted into the transmit data stream. Once this bit has been toggled from a zero to a one, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Bit 6/Line Interface Reset (LIRST). Setting this bit from a zero to a one will initiate an internal reset that resets the clock recovery state machine and recenters the jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.

Bit 7/E1/T1 Select (ETS).
0 = T1 Mode Selected
1 = E1 Mode Selected

Register Name: **LIC3**
Register Description: **Line Interface Control 3**
Register Address: **7Ah**

Bit #	7	6	5	4	3	2	1	0
Name	-	TCES	RCES	MM1	MM0	RSCLKE	TSCLKE	TAOZ
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit Alternate Ones and Zeros (TAOZ). Transmit a …101010… pattern (Customer Disconnect Indication Signal) at TTIP and TRING. The transmission of this data pattern is always timed off of TCLK.
0 = disabled
1 = enabled

Bit 1/Transmit Synchronization G.703 Clock Enable (TSCLKE).
0 = disable 1.544 (T1)/2.048 (E1)MHz transmit synchronization clock
1 = enable 1.544 (T1)/2.048 (E1)MHz transmit synchronization clock

Bit 2/Receive Synchronization G.703 Clock Enable (RSCLKE).
0 = disable 1.544 (T1)/2.048 (E1)MHz synchronization receive mode
1 = enable 1.544 (T1)/2.048 (E1)MHz synchronization receive mode

Bits 3 to 4/Monitor Mode (MM0 to MM1).

MM1	MM0	INTERNAL LINEAR GAIN BOOST (dB)
0	0	Normal operation (no boost)
0	1	20
1	0	26
1	1	32

Bit 5/Receive Clock Edge Select (RCES). Selects which RCLKO edge to update RPOSO and RNEGO.
0 = update RPOSO and RNEGO on rising edge of RCLKO
1 = update RPOSO and RNEGO on falling edge of RCLKO

Bit 6/Transmit Clock Edge Select (TCES). Selects which TCLKI edge to sample TPOSI and TNEGI.
0 = sample TPOSI and TNEGI on falling edge of TCLKI
1 = sample TPOSI and TNEGI on rising edge of TCLKI

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **LIC4**
Register Description: **Line Interface Control 4**
Register Address: **7Bh**

Bit #	7	6	5	4	3	2	1	0
Name	CMIE	CMII	MPS1	MPS0	TT1	TT0	RT1	RT0
Default	0	0	0	0	0	0	0	0

Bits 0 to 1/Receive Termination Select (RT0 to RT1).

RT1	RT0	INTERNAL RECEIVE TERMINATION CONFIGURATION
0	0	Internal Receive-Side Termination Disabled
0	1	Internal Receive-Side 75O Enabled
1	0	Internal Receive-Side 100O Enabled
1	1	Internal Receive-Side 120O Enabled

Bits 2 to 3/Transmit Termination Select (TT0 to TT1).

TT1	TT0	INTERNAL TRANSMIT TERMINATION CONFIGURATION
0	0	Internal Transmit-Side Termination Disabled
0	1	Internal Transmit-Side 75O Enabled
1	0	Internal Transmit-Side 100O Enabled
1	1	Internal Transmit-Side 120O Enabled

Bits 4 and 5/MCLK Prescaler for T1 Mode.

MCLK (MHz)	MPS1	MPS0	JAMUX (LIC2.3)
1.544	0	0	0
3.088	0	1	0
6.176	1	0	0
12.352	1	1	0
2.048	0	0	1
4.096	0	1	1
8.192	1	0	1
16.384	1	1	1

Bits 4 and 5/MCLK Prescaler for E1 Mode.

MCLK (MHz)	MPS1	MPS0	JAMUX (LIC2.3)
2.048	0	0	0
4.096	0	1	0
8.192	1	0	0
16.384	1	1	0

Bit 6/CMI Invert (CMII).
0 = CMI normal at TTIP and RTIP
1 = invert CMI signal at TTIP and RTIP

Bit 7/CMI Enable (CMIE).
0 = disable CMI mode
1 = enable CMI mode

Register Name: **INFO2**
Register Description: **Information Register 2**
Register Address: **11h**

Bit #	7	6	5	4	3	2	1	0
Name	BSYNC	-	TCLE	TOCD	RL3	RL2	RL1	RL0
Default	0	0	0	0	0	0	0	0

Bits 0 to 3/Receive Level Bits (RL0 to RL3). Real-time bits

RL3	RL2	RL1	RL0	RECEIVE LEVEL (dB)
0	0	0	0	Greater than -2.5
0	0	0	1	-2.5 to -5.0
0	0	1	0	-5.0 to -7.5
0	0	1	1	-7.5 to -10.0
0	1	0	0	-10.0 to -12.5
0	1	0	1	-12.5 to -15.0
0	1	1	0	-15.0 to -17.5
0	1	1	1	-17.5 to -20.0
1	0	0	0	-20.0 to -22.5
1	0	0	1	-22.5 to -25.0
1	0	1	0	-25.0 to -27.5
1	0	1	1	-27.5 to -30.0
1	1	0	0	-30.0 to –32.5
1	1	0	1	-32.5 to -35.0
1	1	1	0	-35.0 to -37.5
1	1	1	1	Less than -37.5

Bit 4/Transmit Open Circuit Detect. (TOCD) A real-time bit set when the device detects that the TTIP and TRING outputs are open-circuited.

Bit 5/Transmit Current Limit Exceeded. (TCLE) A real-time bit set when the 50mA (rms) current limiter is activated, whether the current limiter is enabled or not.

Bit 6/Unused.

Bit 7/BERT Real-Time Synchronization Status (BSYNC). Real-time status of the synchronizer (this bit is not latched). Will be set when the incoming pattern matches for 32 consecutive bit positions. Will be cleared when six or more bits out of 64 are received in error. Refer to BSYNC in the BERT status register, SR9, for an interrupt generating version of this signal.

Register Name: **CCR4**
Register Description: **Common Control Register 4**
Register Address: **73h**

Bit #	7	6	5	4	3	2	1	0
Name	RLT3	RLT2	RLT1	RLT0	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 0/Unused, must be set to zero for proper operation.

Bit 1/Unused, must be set to zero for proper operation.

Bit 2/Unused, must be set to zero for proper operation.

Bit 3/Unused, must be set to zero for proper operation.

Bits 4 to 7/Receive Level Threshold Bits (RLT0 to RLT3)

RLT3	RLT2	RLT1	RLT0	Receive Level (dB)
0	0	0	0	Greater than -2.5
0	0	0	1	-2.5
0	0	1	0	-5.0
0	0	1	1	-7.5
0	1	0	0	-10.0
0	1	0	1	-12.5
0	1	1	0	-15.0
0	1	1	1	-17.5
1	0	0	0	-20.0
1	0	0	1	-22.5
1	0	1	0	-25.0
1	0	1	1	-27.5
1	1	0	0	-30.0
1	1	0	1	-32.5
1	1	1	0	-35.0
1	1	1	1	Less than -37.5

Register Name: **SR1**
Register Description: **Status Register 1**
Register Address: **16h**

Bit #	7	6	5	4	3	2	1	0
Name	ILUT	TIMER	RSCOS	JALT	LRCL	TCLE	TOCD	LOLITC
Default	0	0	0	0	0	0	0	0

Bit 0/Loss of Line Interface Transmit Clock Condition (LOLITC). Set when TCLKI has not transitioned for one channel time.

Bit 1/Transmit Open Circuit Detect Condition (TOCD). Set when the device detects that the TTIP and TRING outputs are open-circuited.

Bit 2/Transmit Current Limit Exceeded Condition (TCLE). Set when the 50mA (rms) current limiter is activated whether the current limiter is enabled or not.

Bit 3/Line Interface Receive Carrier Loss Condition (LRCL). Set when the carrier signal is lost.

Bit 4/Jitter Attenuator Limit Trip Event (JALT). Set when the jitter attenuator FIFO reaches to within 4 bits of its useful limit. Will be cleared when read. Useful for debugging jitter-attenuation operation.

Bit 5/Receive Signaling Change Of State Event (RSCOS). Set when any channel selected by the receive-signaling change-of-state interrupt-enable registers (RSCSE1 through RSCSE4) changes signaling state.

Bit 6/Timer Event (TIMER). Follows the error counter update interval as determined by the ECUS bit in the Error Counter Configuration Register (ERCNT).
T1 Mode: Set on increments of one second or 42ms based on RCLK.
E1 Mode: Set on increments of one second or 62.5ms based on RCLK.

Bit 7/Input Level Under Threshold (ILUT). This bit is set whenever the input level at RTIP and RRING falls below the threshold set by the value in CCR4.4 through CCR4.7. The level must remain below the programmed threshold for approximately 50ms for this bit to be set. This is a double interrupt bit.

Register Name: **IMR1**
Register Description: **Interrupt Mask Register 1**
Register Address: **17h**

Bit #	7	6	5	4	3	2	1	0
Name	-	TIMER	RSCOS	JALT	LRCL	TCLE	TOCD	LOLITC
Default	0	0	0	0	0	0	0	0

Bit 0/Loss of Transmit Clock Condition (LOLITC).
0 = interrupt masked
1 = interrupt enabled–generates interrupts on rising and falling edges

Bit 1/Transmit Open Circuit Detect Condition (TOCD).
0 = interrupt masked
1 = interrupt enabled–generates interrupts on rising and falling edges

Bit 2/Transmit Current Limit Exceeded Condition (TCLE).
0 = interrupt masked
1 = interrupt enabled–generates interrupts on rising and falling edges

Bit 3/Line Interface Receive Carrier Loss Condition (LRCL).
0 = interrupt masked
1 = interrupt enabled–generates interrupts on rising and falling edges

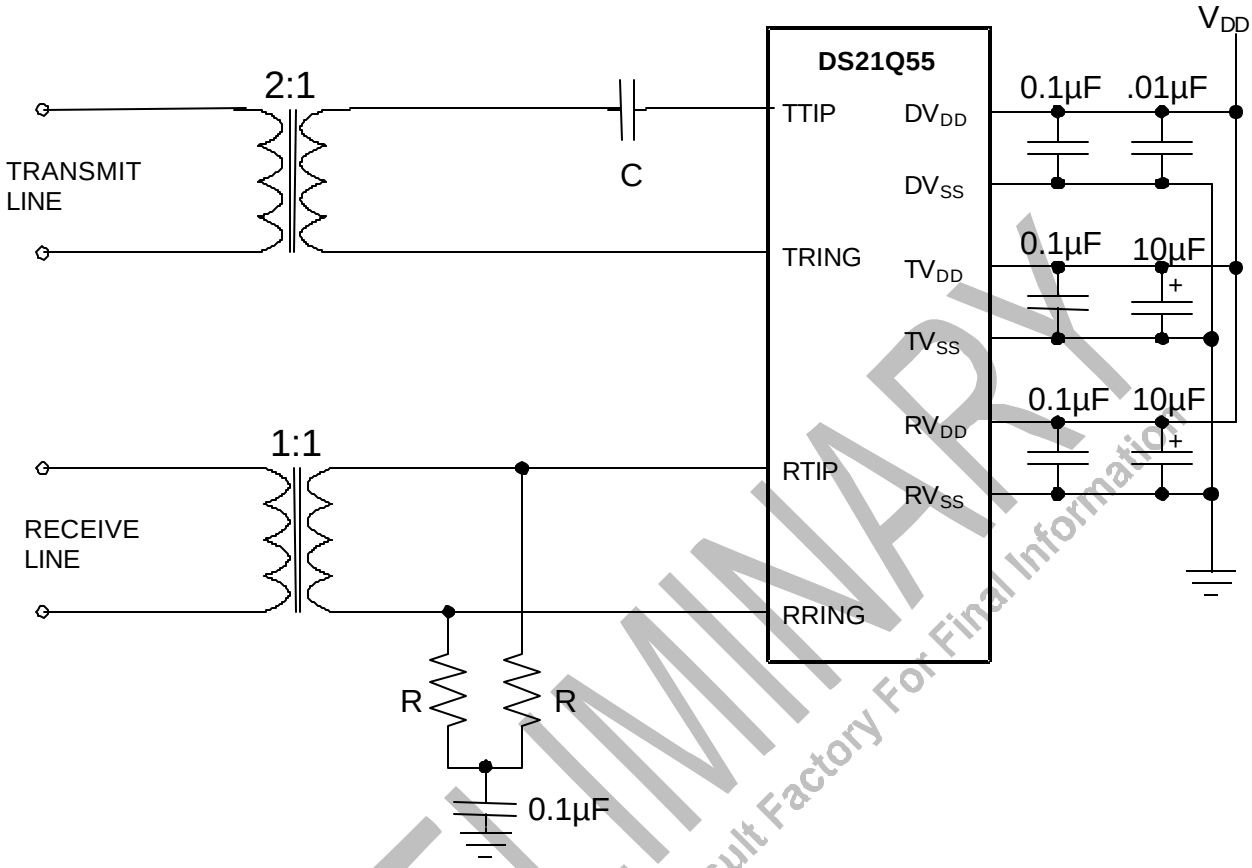
Bit 4/Jitter Attenuator Limit Trip Event (JALT).
0 = interrupt masked
1 = interrupt enabled

Bit 5/Receive Signaling Change Of State Event (RSCOS).
0 = interrupt masked
1 = interrupt enabled

Bit 6/Timer Event (TIMER).
0 = interrupt masked
1 = interrupt enabled

23.8 Recommended Circuits

BASIC INTERFACE Figure 25-4

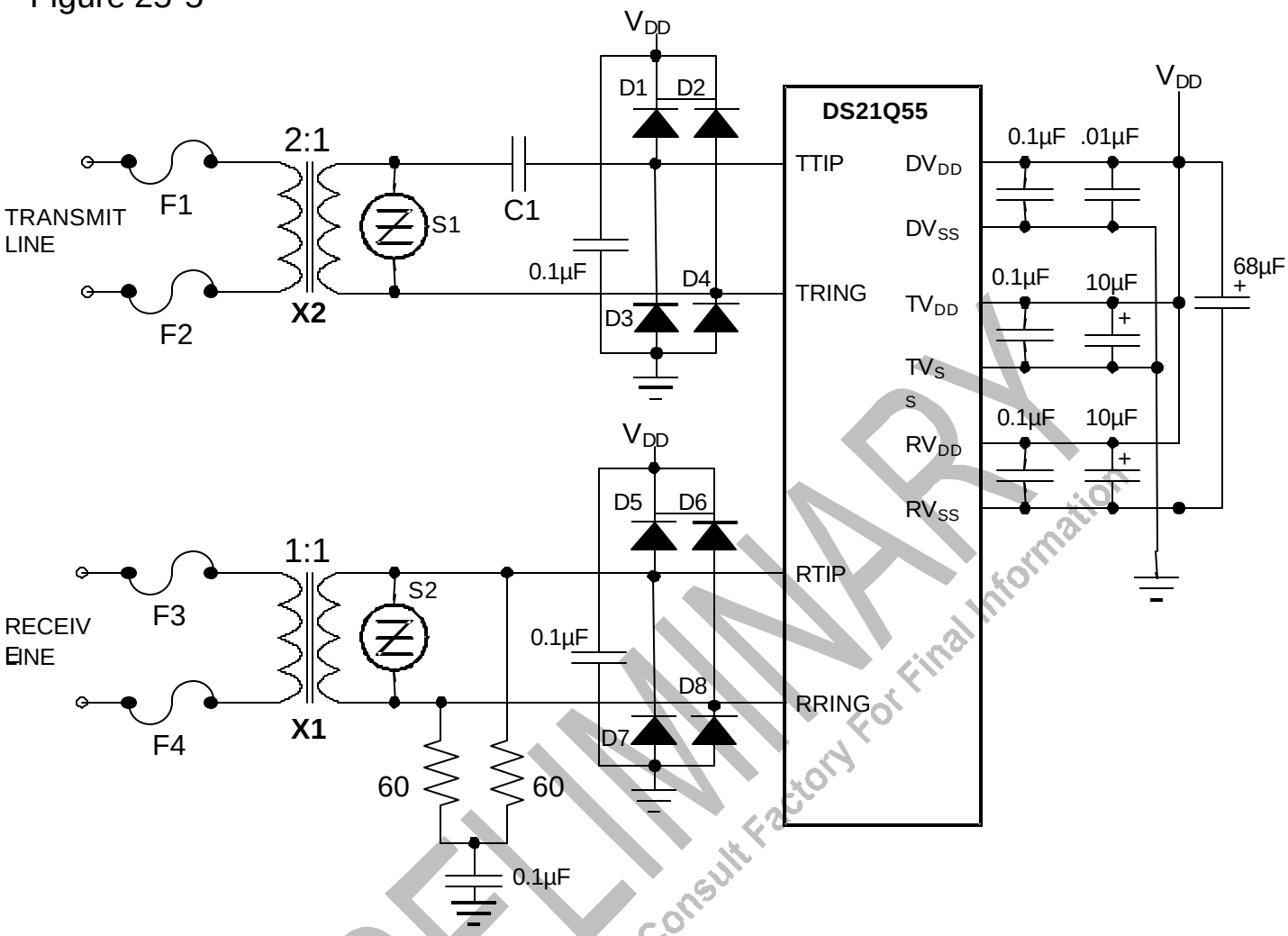


NOTES:

1) All resistor values are ±1%.
2) Resistors R should be set to 60Ω each if the internal receive-side termination feature is enabled. When this feature is disabled, R = 37.5Ω for 75Ω coaxial E1 lines, 60Ω for 120Ω twisted pair E1 lines, or 50Ω for 100Ω twisted pair T1 lines.
3) C = 1µF ceramic.

PROTECTED INTERFACE USING INTERNAL RECEIVE TERMINATION

Figure 25-5



NOTES:

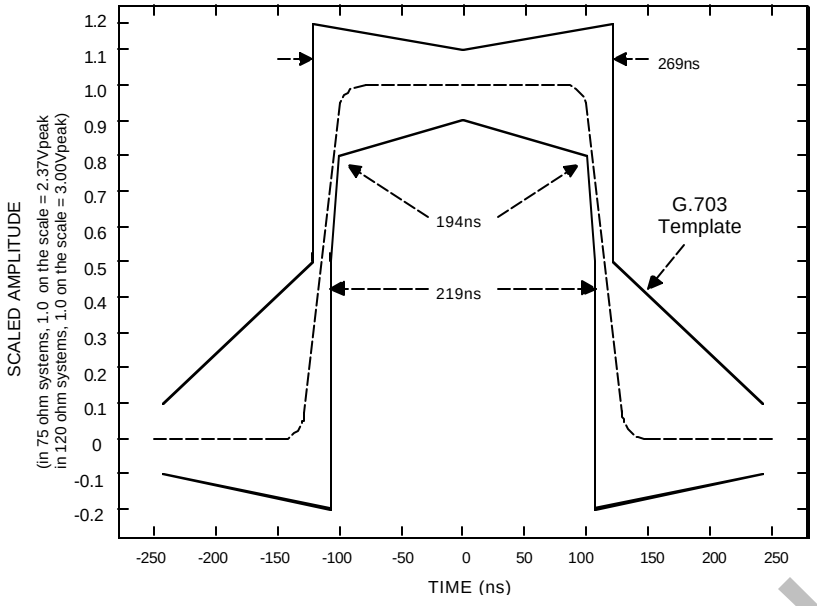
1) All resistor values are ±1%.
2) X1 and X2 are very low DCR transformers
3) C1 = 1µF ceramic.
4) S1 and S2 are 6V transient suppressers.
5) D1 to D8 are Schottky diodes.
6) The fuses, F1–F4, are optional to prevent AC power-line crosses from compromising the transformers.
7) The 68µF is used to keep the local power-plane potential within tolerance during a surge.

23.9 Component Specifications

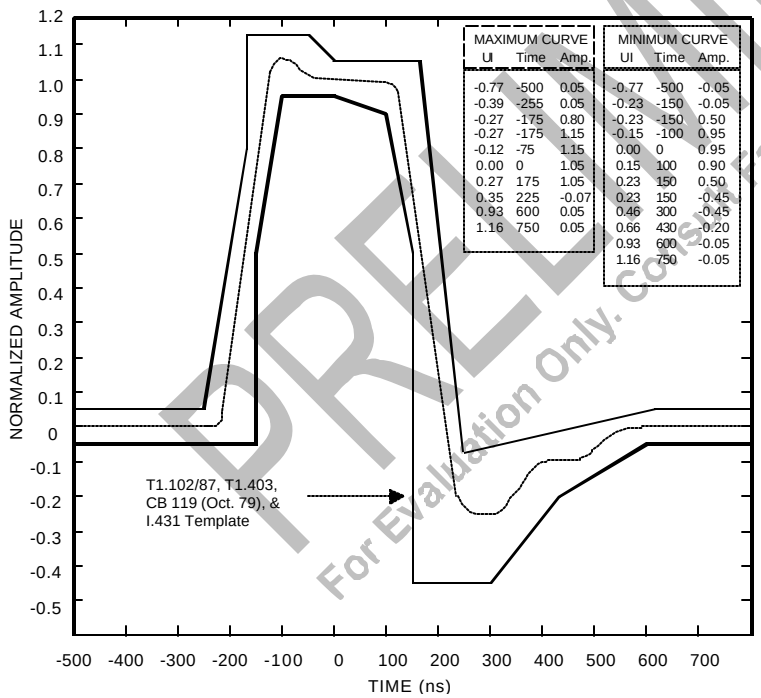
TRANSFORMER SPECIFICATIONS Table 25-1

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio 3.3V Applications	1:1 (receive) and 1:2 (transmit) ±2%
Primary Inductance	600µH minimum
Leakage Inductance	1.0µH maximum
Intertwining Capacitance	40pF maximum
Transmit Transformer DC Resistance Primary (Device Side) Secondary	 1.0O maximum 2.0O maximum
Receive Transformer DC Resistance Primary (Device Side) Secondary	 1.2O maximum 1.2O maximum

E1 TRANSMIT PULSE TEMPLATE Figure 25-6



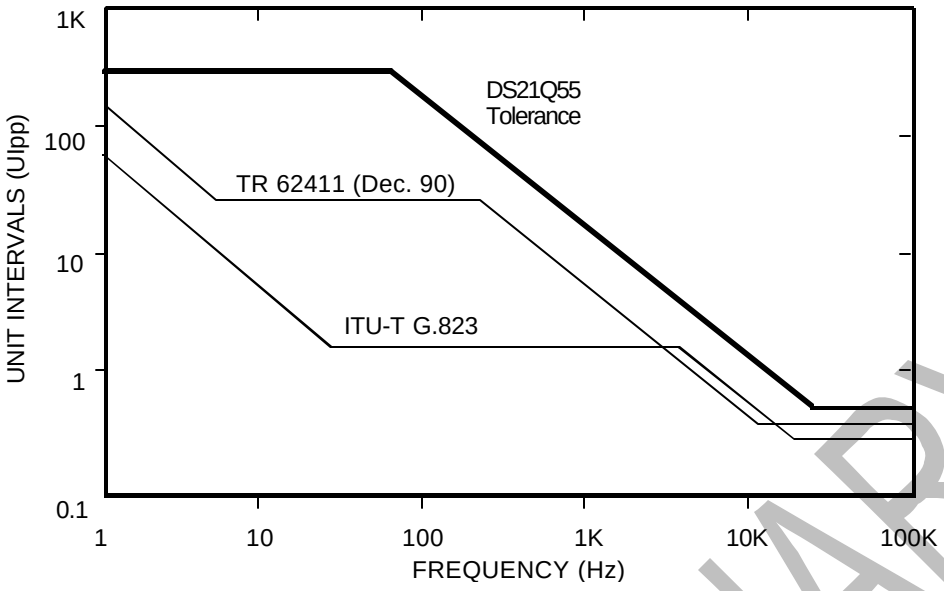
T1 TRANSMIT PULSE TEMPLATE Figure 25-7



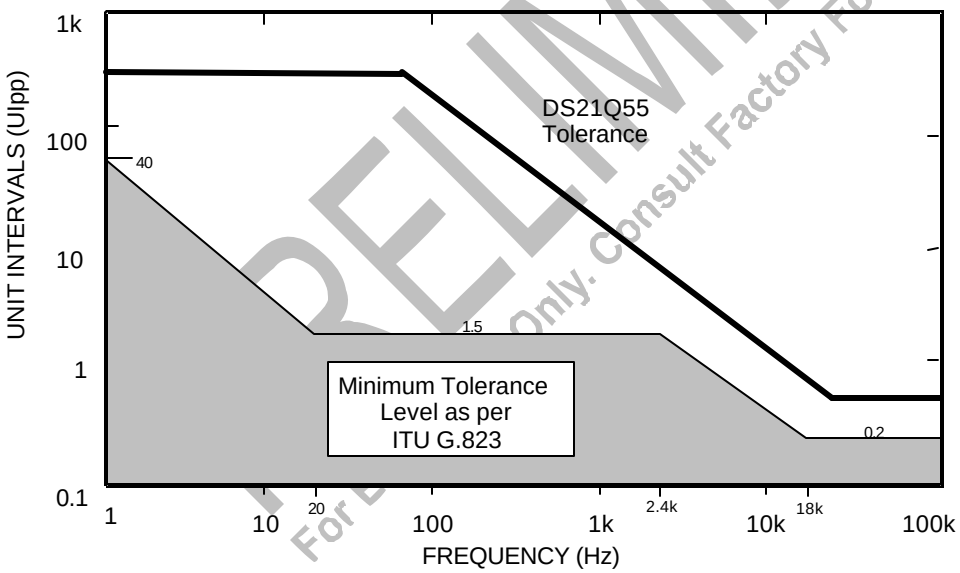
MAXIMUM CURVE		
UI	Time	Amp.
-0.77	-500	0.05
-0.39	-255	0.05
-0.27	-175	0.80
-0.27	-175	1.15
-0.12	-75	1.15
0.00	0	1.05
0.27	175	1.05
0.35	225	-0.07
0.93	600	0.05
1.16	750	0.05

MINIMUM CURVE		
UI	Time	Amp.
-0.77	-500	-0.05
-0.23	-150	-0.05
-0.23	-150	0.50
-0.15	-100	0.95
0.00	0	0.95
0.15	100	0.90
0.23	150	0.50
0.23	150	-0.45
0.46	300	-0.45
0.66	430	-0.20
0.93	600	-0.05
1.16	750	-0.05

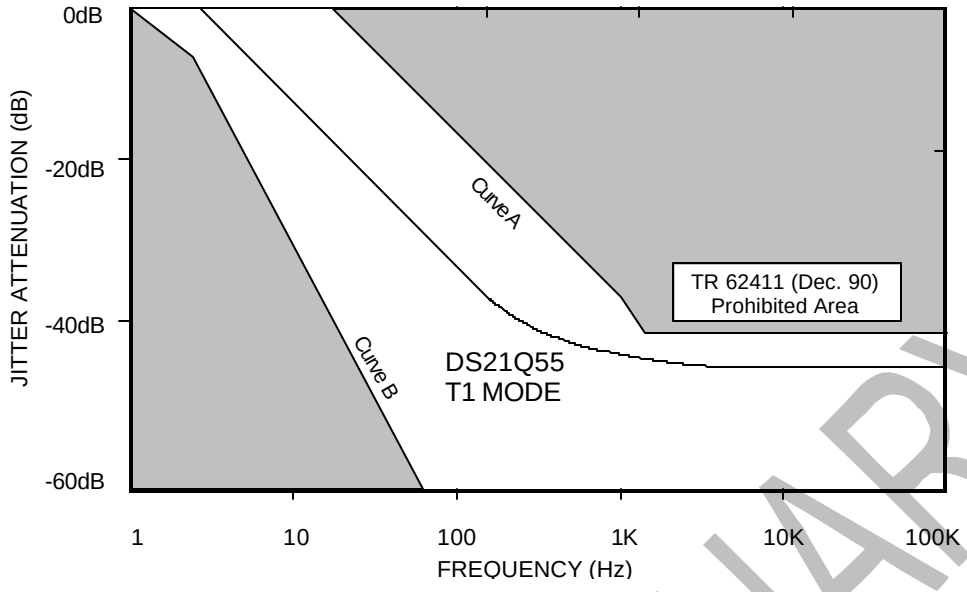
JITTER TOLERANCE (T1 MODE) Figure 25-8



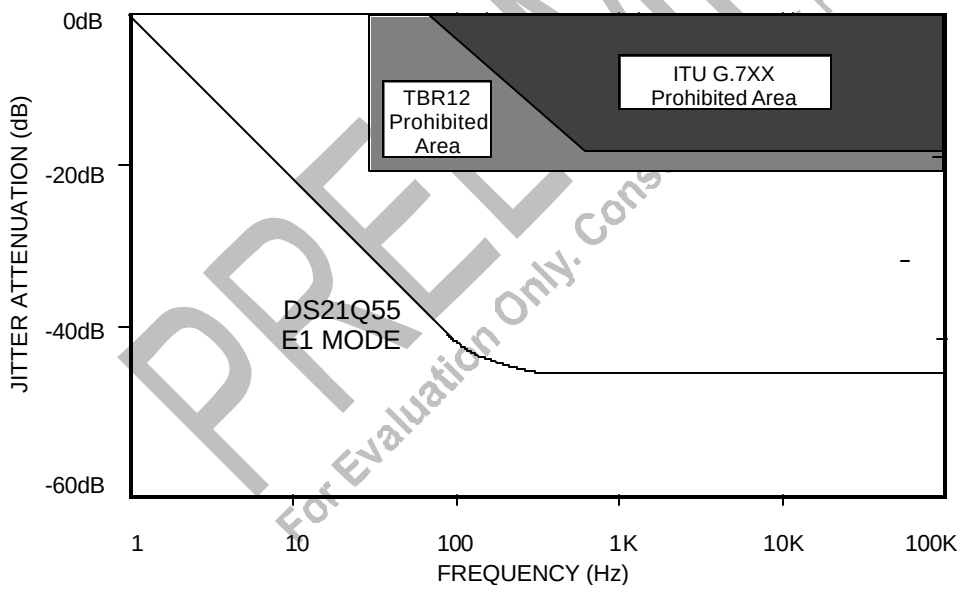
JITTER TOLERANCE (E1 MODE) Figure 25-9



JITTER ATTENUATION (T1 MODE) Figure 25-10



JITTER ATTENUATION (E1 MODE) Figure 25-11



24. PROGRAMMABLE IN-BAND LOOP CODE GENERATION AND DETECTION

The DS21Q55 has the ability to generate and detect a repeating bit pattern from 1 bit to 8 bits or 16 bits in length. **This function is available only in T1 mode**. To transmit a pattern, the user will load the pattern to be sent into the transmit code definition registers (TCD1 and TCD2) and select the proper length of the pattern by setting the TC0 and TC1 bits in the in-band code-control (IBCC) register. When generating a 1-, 2-, 4-, 8-, or 16-bit pattern both transmit code-definition registers (TCD1 and TCD2) must be filled with the proper code. Generation of a 3-, 5-, 6-, and 7-bit pattern only requires TCD1 to be filled. Once this is accomplished, the pattern will be transmitted as long as the TLOOP control bit (T1CCR1.0) is enabled. Normally (unless the transmit formatter is programmed to not insert the F-bit position) the framer will overwrite the repeating pattern once every 193 bits to allow the F-bit position to be sent.

An example: to transmit the standard loop-up code for channel service units (CSUs), which is a repeating pattern of ...10000100001..., set TCD1 = 80h, IBCC = 0 and T1CCR1.0 = 1.

The framer has three programmable pattern detectors. Typically, two of the detectors are used for loop-up and loop-down code detection. The user will program the codes to be detected in the receive-up code-definition (RUPCD1 and RUPCD2) registers and the receive-down code-definition (RDNCD1 and RDNCD2) registers and the length of each pattern will be selected via the IBCC register. A third detector (spare) is defined and controlled via the RSCD1/RSCD2 and RSCC registers. Both receive code-definition registers are used together to form a 16-bit register when detecting a 16-bit pattern. Both receive code-definition registers will be filled with the same value for 8-bit patterns. Detection of a 1-, 2-, 3-, 4-, 5-, 6-, and 7-bit pattern only requires the first receive code-definition register to be filled. The framer will detect repeating pattern codes in both framed and unframed circumstances with bit error rates as high as 10E-2. The detectors are capable of handling both F-bit inserted and F-bit overwrite patterns. Writing the least significant byte of the receive code-definition register resets the integration period for that detector. The code detector has a nominal integration period of 36ms. Hence, after about 36ms of receiving a valid code, the proper status bit (LUP at SR3.5, LDN at SR3.6, and LSPARE at SR3.7) will be set to a one. Normally codes are sent for a period of five seconds. It is recommended that the software poll the framer every 50ms to 1000ms until five seconds has elapsed to ensure that the code is continuously present.

Register Name: **IBCC**
Register Description: **In-Band Code Control Register**
Register Address: **B6h**

Bit #	7	6	5	4	3	2	1	0
Name	TC1	TC0	RUP2	RUP1	RUP0	RDN2	RDN1	RDN0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2/Receive -Down Code Length Definition Bits (RDN0 to RDN2).

RDN2	RDN1	RDN0	LENGTH SELECTED (Bits)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8/16

Bits 3 to 5/Receive -Up Code Length Definition Bits (RUP0 to RUP2).

RUP2	RUP1	RUP0	LENGTH SELECTED (Bits)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8/16

Bits 6 to 7/Transmit Code Length Definition Bits (TC0 to TC1).

TC1	TC0	LENGTH SELECTED (Bits)
0	0	5
0	1	6/3
1	0	7
1	1	16/8/4/2/1

Register Name: **TCD1**
Register Description: **Transmit Code Definition Register 1**
Register Address: **B7h**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit Code Definition Bit 0 (C0). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 1/Transmit Code Definition Bit 1 (C1). A “don’t care” if a 5-bit or 6-bit length is selected.

Bit 2/Transmit Code Definition Bit 2 (C2). A “don’t care” if a 5-bit length is selected.

Bit 3/Transmit Code Definition Bit 3 (C3).

Bit 4/Transmit Code Definition Bit 4 (C4).

Bit 5/Transmit Code Definition Bit 5 (C5).

Bit 6/Transmit Code Definition Bit 6 (C6).

Bit 7/Transmit Code Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **TCD2**
Register Description: **Transmit Code Definition Register 2**
Register Address: **B8h**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Note: Least significant byte of 16-bit codes

Bit 0/Transmit Code Definition Bit 0 (C0). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 1/Transmit Code Definition Bit 1 (C1). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 2/Transmit Code Definition Bit 2 (C2). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 3/Transmit Code Definition Bit 3 (C3). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 4/Transmit Code Definition Bit 4 (C4). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 5/Transmit Code Definition Bit 5 (C5). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 6/Transmit Code Definition Bit 6 (C6). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Bit 7/Transmit Code Definition Bit 7 (C7). A “don’t care” if a 5-, 6-, or 7-bit length is selected.

Register Name: **RUPCD1**
Register Description: **Receive-Up Code Definition Register 1**
Register Address: **B9h**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Note: Writing this register resets the detector's integration period.

Bit 0/Receive-Up Code Definition Bit 0 (C0). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 1/Receive-Up Code Definition Bit 1 (C1). A "don't care" if a 1-bit to 6-bit length is selected.

Bit 2/Receive-Up Code Definition Bit 2 (C2). A "don't care" if a 1-bit to 5-bit length is selected.

Bit 3/Receive-Up Code Definition Bit 3 (C3). A "don't care" if a 1-bit to 4 bit length is selected.

Bit 4/Receive-Up Code Definition Bit 4 (C4). A "don't care" if a 1-bit to 3-bit length is selected.

Bit 5/Receive-Up Code Definition Bit 5 (C5). A "don't care" if a 1-bit or 2-bit length is selected.

Bit 6/Receive-Up Code Definition Bit 6 (C6). A "don't care if a 1-bit length is selected.

Bit 7/Receive-Up Code Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **RUPCD2**
Register Description: **Receive-Up Code Definition Register 2**
Register Address: **Bah**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0/Receive-Up Code Definition Bit 0 (C0). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 1/Receive-Up Code Definition Bit 1 (C1). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 2/Receive-Up Code Definition Bit 2 (C2). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 3/Receive-Up Code Definition Bit 3 (C3). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 4/Receive-Up Code Definition Bit 4 (C4). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 5/Receive-Up Code Definition Bit 5 (C5). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 6/Receive-Up Code Definition Bit 6 (C6). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 7/Receive-Up Code Definition Bit 7 (C7). A "don't care" if a 1-bit to 7-bit length is selected.

Register Name: **RDNCD1**
Register Description: **Receive-Down Code Definition Register 1**
Register Address: **BBh**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Note: Writing this register resets the detector's integration period.

Bit 0/Receive-Down Code Definition Bit 0 (C0). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 1/Receive-Down Code Definition Bit 1 (C1). A "don't care" if a 1-bit to 6-bit length is selected.

Bit 2/Receive-Down Code Definition Bit 2 (C2). A "don't care" if a 1-bit to 5-bit length is selected.

Bit 3/Receive-Down Code Definition Bit 3 (C3). A "don't care" if a 1-bit to 4-bit length is selected.

Bit 4/Receive-Down Code Definition Bit 4 (C4). A "don't care" if a 1-bit to 3-bit length is selected.

Bit 5/Receive-Down Code Definition Bit 5 (C5). A "don't care" if a 1-bit or 2-bit length is selected.

Bit 6/Receive-Down Code Definition Bit 6 (C6). A "don't care" if a 1-bit length is selected.

Bit 7/Receive-Down Code Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **RDNCD2**
Register Description: **Receive-Down Code Definition Register 2**
Register Address: **BCh**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0/Receive-Down Code Definition Bit 0 (C0). A “don’t care” if a 1-bit to 7-bit length is selected.

Bit 1/Receive-Down Code Definition Bit 1 (C1). A “don’t care” if a 1-bit to 7-bit length is selected.

Bit 2/Receive-Down Code Definition Bit 2 (C2). A “don’t care” if a 1-bit to 7-bit length is selected.

Bit 3/Receive-Down Code Definition Bit 3 (C3). A “don’t care” if a 1-bit to 7-bit length is selected.

Bit 4/Receive-Down Code Definition Bit 4 (C4). A “don’t care” if a 1-bit to 7-bit length is selected.

Bit 5/Receive-Down Code Definition Bit 5 (C5). A “don’t care” if a 1-bit to 7-bit length is selected.

Bit 6/Receive-Down Code Definition Bit 6 (C6). A “don’t care” if a 1-bit to 7-bit length is selected.

Bit 7/Receive-Down Code Definition Bit 7 (C7). A “don’t care” if a 1-bit to 7-bit length is selected.

Register Name: **RSCC**
Register Description: **In-Band Receive Spare Control Register**
Register Address: **BDh**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	RSC2	RSC1	RSC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2/Receive Spare Code Length Definition Bits (RSC0 to RSC2).

RSC2	RSC1	RSC0	LENGTH SELECTED (Bits)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8/16

Bit 3/Unused, must be set to zero for proper operation.

Bit 4/Unused, must be set to zero for proper operation.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **RSCD1**
Register Description: **Receive-Spare Code Definition Register 1**
Register Address: **BEh**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Note: Writing this register resets the detector's integration period.

Bit 0/Receive-Spare Code Definition Bit 0 (C0). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 1/Receive-Spare Code Definition Bit 1 (C1). A "don't care" if a 1-bit to 6-bit length is selected.

Bit 2/Receive-Spare Code Definition Bit 2 (C2). A "don't care" if a 1-bit to 5-bit length is selected.

Bit 3/Receive-Spare Code Definition Bit 3 (C3). A "don't care" if a 1-bit to 4-bit length is selected

Bit 4/Receive-Spare Code Definition Bit 4 (C4). A "don't care" if a 1-bit to 3-bit length is selected.

Bit 5/Receive-Spare Code Definition Bit 5 (C5). A "don't care" if a 1-bit or 2-bit length is selected.

Bit 6/Receive-Spare Code Definition Bit 6 (C6). A "don't care" if a 1-bit length is selected.

Bit 7/Receive-Spare Code Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **RSCD2**
Register Description: **Receive-Spare Code Definition Register 2**
Register Address: **BFh**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0/Receive-Spare Code Definition Bit 0 (C0). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 1/Receive-Spare Code Definition Bit 1 (C1). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 2/Receive-Spare Code Definition Bit 2 (C2). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 3/Receive-Spare Code Definition Bit 3 (C3). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 4/Receive-Spare Code Definition Bit 4 (C4). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 5/Receive-Spare Code Definition Bit 5 (C5). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 6/Receive-Spare Code Definition Bit 6 (C6). A "don't care" if a 1-bit to 7-bit length is selected.

Bit 7/Receive-Spare Code Definition Bit 7 (C7). A "don't care" if a 1-bit to 7-bit length is selected.

25. BERT FUNCTION

The BERT (Bit Error Rate Tester) block can generate and detect both pseudorandom and repeating-bit patterns. It is used to test and stress data-communication links.

The BERT block is capable of generating and detecting the following patterns:

- The pseudorandom patterns 2E7, 2E11, 2E15, and QR_{SS}
- A repetitive pattern from 1 to 32 bits in length
- Alternating (16-bit) words that flip every 1 to 256 words
- Daly pattern

The BERT function is assigned on a per-channel basis for both the transmitter and receiver. This is accomplished by using the special per-channel function. Using this function, the BERT pattern can be transmitted and/or received in single or across multiple DS0s, contiguous or broken. Transmit and receive bandwidth assignments are independent of each other.

The BERT receiver has a 32-bit bit counter and a 24-bit error counter. The BERT receiver will report three events: a change in receive-synchronizer status, a bit error detection, and if either the bit counter or the error counter overflows. Each of these events can be masked within the BERT function via the BERT control register 1 (BC1). If the software detects that the BERT has reported an event, then the software must read the BERT information register (BIR) to determine which event(s) has occurred. To activate the BERT block, the host must configure the BERT multiplexer via the BIC register.

SR9 contains the status information on the BERT function. The host can be alerted when there is a change of state of the BERT via this register. A major change of state is defined as either a change in the receive synchronization (i.e., the BERT has gone into or out of receive synchronization), a bit error has been detected, or an overflow has occurred in either the bit counter or the error counter. The host must read SR9 to determine the change of state.

25.1 BERT Register Description

Register Name: **BC1**
Register Description: **BERT Control Register 1**
Register Address: **E0h**

Bit #	7	6	5	4	3	2	1	0
Name	TC	TINV	RINV	PS2	PS1	PS0	LC	RESYNC
Default	0	0	0	0	0	0	0	0

Bit 0/Force Resynchronization (RESYNC). A low-to-high transition will force the receive BERT synchronizer to resynchronize to the incoming data stream. This bit should be toggled from low to high whenever the host wishes to acquire synchronization on a new pattern. Must be cleared and set again for a subsequent resynchronization.

Bit 1/Load Bit and Error Counters (LC). A low-to-high transition latches the current bit and error counts into the registers BBC1/BBC2/BBC3/BBC4 and BEC1/BEC2/BEC3 and clears the internal count. This bit should be toggled from low to high whenever the host wishes to begin a new acquisition period. Must be cleared and set again for a subsequent loads.

Bits 2 to 4/Pattern Select Bits (PS0 to PS2)

PS2	PS1	PS0	PATTERN DEFINITION
0	0	0	Pseudorandom 2E7–1
0	0	1	Pseudorandom 2E11–1
0	1	0	Pseudorandom 2E15–1
0	1	1	Pseudorandom Pattern QR_{SS}. A 2^{20} - 1 pattern with 14 consecutive zero estriction.
1	0	0	Repetitive Pattern
1	0	1	Alternating Word Pattern
1	1	0	Modified 55 Octet (Daly) Pattern The Daly pattern is a repeating 55 octet pattern that is byte-aligned into the active DS0 timeslots. The pattern is defined in an ATIS (Alliance for Telecommunications Industry Solutions) Committee T1 Technical Report Number 25 (November 1993).
1	1	1	Reserved

Bit 5/Receive Invert Data Enable (RINV).
0 = do not invert the incoming data stream
1 = invert the incoming data stream

Bit 6/Transmit Invert Data Enable (TINV).
0 = do not invert the outgoing data stream
1 = invert the outgoing data stream

Bit 7/Transmit Pattern Load (TC). A low-to-high transition loads the pattern generator with the pattern that is to be generated. This bit should be toggled from low to high whenever the host wishes to load a new pattern. Must be cleared and set again for a subsequent loads.

Register Name: **BC2**
Register Description: **BERT Control Register 2**
Register Address: **E1h**

Bit #	7	6	5	4	3	2	1	0
Name	EIB2	EIB1	EIB0	SBE	RPL3	RPL2	RPL1	RPL0
Default	0	0	0	0	0	0	0	0

Bits 0 to 3/Repetitive Pattern Length Bit 3 (RPL0 to RPL3). RPL0 is the LSB and RPL3 is the MSB of a nibble that describes the how long the repetitive pattern is. The valid range is 17 (0000) to 32 (1111). These bits are ignored if the receive BERT is programmed for a pseudorandom pattern. To create repetitive patterns less than 17 bits in length, the user must set the length to an integer number of the desired length that is less than or equal to 32. For example, to create a 6-bit pattern, the user can set the length to 18 (0001) or to 24 (0111) or to 30 (1101).

Length (Bits)	RPL3	RPL2	RPL1	RPL0
17	0	0	0	0
18	0	0	0	1
19	0	0	1	0
20	0	0	1	1
21	0	1	0	0
22	0	1	0	1
23	0	1	1	0
24	0	1	1	1
25	1	0	0	0
26	1	0	0	1
27	1	0	1	0
28	1	0	1	1
29	1	1	0	0
30	1	1	0	1
31	1	1	1	0
32	1	1	1	1

Bit 4/Single Bit Error Insert (SBE). A low-to-high transition will create a single bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bits 5 to 7/Error Insert Bits 0 to 2 (EIB0 to EIB2). Will automatically insert bit errors at the prescribed rate into the generated data pattern. Can be used for verifying error detection features.

EIB2	EIB1	EIB0	ERROR RATE INSERTED
0	0	0	No errors automatically inserted
0	0	1	10E-1
0	1	0	10E-2
0	1	1	10E-3
1	0	0	10E-4
1	0	1	10E-5
1	1	0	10E-6
1	1	1	10E-7

Register Name: **BIC**
Register Description: **BERT Interface Control Register**
Register Address: **EAh**

Bit #	7	6	5	4	3	2	1	0
Name	-	RFUS	-	TBAT	TFUS	-	BERTDIR	BERTEN
Default	0	0	0	0	0	0	0	0

Bit 0/BERT Enable (BERTEN).
0 = BERT disabled
1 = BERT enabled

Bit 1/BERT Direction (BERTDIR).
0 = network
1 = system

Bit 2/Unused, must be set to zero for proper operation.

Bit 3/Transmit Framed/Unframed Select (TFUS). For T1 mode only.
0 = BERT will not source data into the F-bit position (framed)
1 = BERT will source data into the F-bit position (unframed)

Bit 4/Transmit Byte Align Toggle (TBAT). A zero-to-one transition will force the BERT to byte align its pattern with the transmit formatter. This bit must be transitioned in order to byte-align the Daly Pattern.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Receive Framed/Unframed Select (RFUS). For T1 mode only.
0 = BERT will not sample data from the F-bit position (framed)
1 = BERT will sample data from the F-bit position (unframed)

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **SR9**
Register Description: **Status Register 9**
Register Address: **26h**

Bit #	7	6	5	4	3	2	1	0
Name	-	BBED	BBCO	BEC0	BRA1	BRA0	BRLOS	BSYNC
Default	0	0	0	0	0	0	0	0

Bit 0/BERT in Synchronization Condition (BSYNC). Will be set when the incoming pattern matches for 32 consecutive bit positions. Refer to BSYNC in INFO2 register for a real-time version of this bit.

Bit 1/BERT Receive Loss Of Synchronization Condition (BRLOS). A latched bit that is set whenever the receive BERT begins searching for a pattern. The BERT will lose sync after receiving six errored bits out of 63 bits. Synchronization is lost when six errors are received in 63 bits. Once synchronization is achieved, this bit will remain set until read.

Bit 2/BERT Receive All Zeros Condition (BRA0). A latched bit that is set when 32 consecutive zeros are received. Allowed to be cleared once a one is received.

Bit 3/BERT Receive All Ones Condition (BRA1). A latched bit that is set when 32 consecutive ones are received. Allowed to be cleared once a zero is received.

Bit 4/BERT Error Counter Overflow (BECO) Event (BECO). A latched bit that is set when the 24-bit BERT error counter (BEC) overflows. Cleared when read and will not be set again until another overflow occurs.

Bit 5/BERT Bit Counter Overflow Event (BBCO). A latched bit that is set when the 32-bit BERT bit counter (BBC) overflows. Cleared when read and will not be set again until another overflow occurs.

Bit 6/BERT Bit Error Detected (BED) Event (BBED). A latched bit that is set when a bit error is detected. The receive BERT must be in synchronization for it detect bit errors. Cleared when read.

Register Name: **IMR9**
Register Description: **Interrupt Mask Register 9**
Register Address: **27h**

Bit #	7	6	5	4	3	2	1	0
Name	-	BBED	BBCO	BEC0	BRA1	BRA0	BRLOS	BSYNC
Default	0	0	0	0	0	0	0	0

Bit 0/BERT in Synchronization Condition (BSYNC).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 1/Receive Loss Of Synchronization Condition (BRLOS).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 2/Receive All Zeros Condition (BRA0).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 3/Receive All Ones Condition (BRA1).
0 = interrupt masked
1 = interrupt enabled–interrupts on rising and falling edges

Bit 4/BERT Error Counter Overflow Event (BECO).
0 = interrupt masked
1 = interrupt enabled

Bit 5/BERT Bit Counter Overflow Event (BBCO).
0 = interrupt masked
1 = interrupt enabled

Bit 6/Bit Error Detected Event (BBED).
0 = interrupt masked
1 = interrupt enabled

BERT Alternating Word Count Rate. When the BERT is programmed in the alternating word mode, the words will repeat for the count loaded into this register then flip to the other word and again repeat for the number of times loaded into this register

Register Name: **BAWC**
Register Description: **BERT Alternating Word Count Rate**
Register Address: **DBh**

Bit #	7	6	5	4	3	2	1	0
Name	ACNT7	ACNT6	ACNT5	ACNT4	ACNT3	ACNT2	ACNT1	ACNT0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Alternating Word Count Rate Bits 0 to 7 (ACNT0 to ACNT7). ACNT0 is the LSB of the 8-bit alternating word count rate counter.

25.2 BERT Repetitive Pattern Set

These registers must be properly loaded for the BERT to generate and synchronize to a repetitive pattern, a pseudorandom pattern, alternating word pattern, or a Daly pattern. For a repetitive pattern that is less than 32 bits, the pattern should be repeated so that all 32 bits are used to describe the pattern. For example, if the pattern was the repeating 5-bit pattern …01101… (where the right-most bit is the one sent first and received first) then BRP1 should be loaded with ADh, BRP2 with B5h, BRP3 with D6h, and BRP4 should be loaded with 5Ah. For a pseudorandom pattern, all four registers should be loaded with all ones (i.e., FFh). For an alternating word pattern, one word should be placed into BRP1 and BRP2 and the other word should be placed into BRP3 and BRP4. For example, if the DDS stress pattern "7E" is to be described, the user would place 00h in BRP1, 00h in BRP2, 7Eh in BRP3, and 7Eh in BRP4, and the alternating word counter would be set to 50 (decimal) to allow 100 bytes of 00h followed by 100 bytes of 7Eh to be sent and received.

Register Name: **BRP1**
Register Description: **BERT Repetitive Pattern Set Register 1**
Register Address: **DCh**

Bit #	7	6	5	4	3	2	1	0
Name	RPAT7	RPAT6	RPAT5	RPAT4	RPAT3	RPAT2	RPAT1	RPAT0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Repetitive Pattern Set Bits 0 to 7 (RPAT0 to RPAT7). RPAT0 is the LSB of the 32-bit repetitive pattern set.

Register Name: **BRP2**
Register Description: **BERT Repetitive Pattern Set Register 2**
Register Address: **DDh**

Bit #	7	6	5	4	3	2	1	0
Name	RPAT15	RPAT14	RPAT13	RPAT12	RPAT11	RPAT10	RPAT9	RPAT8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Repetitive Pattern Set Bits 8 to 15 (RPAT8 to RPAT15).

Register Name: **BRP3**
Register Description: **BERT Repetitive Pattern Set Register 3**
Register Address: **DEh**

Bit #	7	6	5	4	3	2	1	0
Name	RPAT23	RPAT22	RPAT21	RPAT20	RPAT19	RPAT18	RPAT17	RPAT16
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Repetitive Pattern Set Bits 16 to 23 (RPAT16 to RPAT23).

Register Name: **BRP4**
Register Description: **BERT Repetitive Pattern Set Register 4**
Register Address: **DFh**

Bit #	7	6	5	4	3	2	1	0
Name	RPAT31	RPAT30	RPAT29	RPAT28	RPAT27	RPAT26	RPAT25	RPAT24
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Repetitive Pattern Set Bits 24 to 31 (RPAT24 to RPAT31). RPAT31 is the LSB of the 32-bit repetitive pattern set.

25.3 BERT Bit Counter

Once BERT has achieved synchronization, this 32-bit counter will increment for each data bit (i.e., clock) received. Toggling the LC control bit in BC1 can clear this counter, which saturates when full and will set the BBCO status bit.

Register Name: **BBC1**
Register Description: **BERT Bit Count Register 1**
Register Address: **E3h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC7	BBC6	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Bit Counter Bits 0 to 7 (BBC0 to BBC7). BBC0 is the LSB of the 32-bit counter.

Register Name: **BBC2**
Regis ter Description: **BERT Bit Count Register 2**
Register Address: **E4h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC15	BBC14	BBC13	BBC12	BBC11	BBC10	BBC9	BBC8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Bit Counter Bits 8 to 15 (BBC8 to BBC15).

Register Name: **BBC3**
Register Description: **BERT Bit Count Register 3**
Register Address: **E5h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC23	BBC22	BBC21	BBC20	BBC19	BBC18	BBC17	BBC16
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Bit Counter Bits 16 to 23 (BBC16 to BBC23).

Register Name: **BBC4**
Register Description: **BERT Bit Count Register 4**
Register Address: **E6h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC31	BBC30	BBC29	BBC28	BBC27	BBC26	BBC25	BBC24
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/BERT Bit Counter Bits 24 to 31 (BBC24 to BBC31). BBC31 is the MSB of the 32-bit counter.

25.4 BERT Error Counter

Once BERT has achieved synchronization, this 24-bit counter will increment for each data bit received in error. Toggling the LC control bit in BC1 can clear this counter. This counter saturates when full and will set the BECO status bit.

Register Name: **BEC1**
Register Description: **BERT Error Count Register 1**
Register Address: **E7h**

Bit #	7	6	5	4	3	2	1	0
Name	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Error Counter Bits 0 to 7 (EC0 to EC7). EC0 is the LSB of the 24-bit counter.

Register Name: **BEC2**
Register Description: **BERT Error Count Register 2**
Register Address: **E8h**

Bit #	7	6	5	4	3	2	1	0
Name	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Error Counter Bits 8 to 15 (EC8 to EC15).

Register Name: **BEC3**
Register Description: **BERT Error Count Register 3**
Register Address: **E9h**

Bit #	7	6	5	4	3	2	1	0
Name	EC23	EC22	EC21	EC20	EC19	EC18	EC17	EC16
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Error Counter Bits 16 to 23 (EC16 to EC23). EC23 is the MSB of the 24-bit counter.

26. PAYLOAD ERROR INSERTION FUNCTION

An error-insertion function is available in the DS21Q55 and is used to create errors in the payload portion of the T1 frame in the transmit path. Errors can be inserted over the entire frame or on a per-channel basis. The user can select all DS0s or any combination of DS0s. See *Special Per-Channel Registration Operation* for information on using the per-channel function. Errors are created by inverting the last bit in the count sequence. For example, if the error rate 1 in 16 is selected, the 16th bit is inverted. F-bits are excluded from the count and are never corrupted. Error rate changes occur on frame boundaries. Error-insertion options include continuous and absolute number with both options supporting selectable-insertion rates.

TRANSMIT ERROR INSERTION SETUP SEQUENCE Table 28-1

STEP	ACTION
1	Enter desired error rate in the ERC register. Note: If ER3 through ER0 = 0, no errors will be generated even if the constant error insertion feature is enabled.
2A or 2B	For constant error insertion set CE = 1 (ERC.4). For a defined number of errors: – Set CE = 0 (ERC.4) – Load NOE1 and NOE2 with the number of errors to be inserted – Toggle WNOE (ERC.7) from 0 to 1, to begin error insertion

Register Name: **ERC**
Register Description: **Error Rate Control Register**
Register Address: **EBh**

Bit #	7	6	5	4	3	2	1	0
Name	WNOE	-	-	CE	ER3	ER2	ER1	ER0
Default	0	0	0	0	0	0	0	0

Bits 0 to 3/Error Insertion Rate Select Bits (ER0 to ER3).

ER3	ER2	ER1	ER0	ERROR RATE
0	0	0	0	No errors inserted
0	0	0	1	1 in 16
0	0	1	0	1 in 32
0	0	1	1	1 in 64
0	1	0	0	1 in 128
0	1	0	1	1 in 256
0	1	1	0	1 in 512
0	1	1	1	1 in 1024
1	0	0	0	1 in 2048
1	0	0	1	1 in 4096
1	0	1	0	1 in 8192
1	0	1	1	1 in 16384
1	1	0	0	1 in 32768
1	1	0	1	1 in 65536
1	1	1	0	1 in 131072
1	1	1	1	1 in 262144

Bit 4/Constant Errors (CE). When this bit is set high (and the ER0 to ER3 bits are not set to 0000), the error insertion logic will ignore the number of error registers (NOE1, NOE2) and generate errors constantly at the selected insertion rate. When CE is set to zero, the NOEx registers determine how many errors are to be inserted.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Write NOE Registers (WNOE). If the host wishes to update to the NOEx registers, this bit must be toggled from a zero to a one after the host has already loaded the prescribed error count into the NOEx registers. The toggling of this bit causes the error count loaded into the NOEx registers to be loaded into the error insertion circuitry on the next clock cycle. Subsequent updates require that the WNOE bit be set to zero and then one once again.

26.1 Number Of Error Registers

The number of error registers determine how many errors will be generated. Up to 1023 errors can be generated. The host will load the number of errors to be generated into the NOE1 and NOE2 registers. The host can also update the number of errors to be created by first loading the prescribed value into the NOE registers and then toggling the WNOE bit in the error rate control registers.

ERROR INSERTION EXAMPLES Table 28-2

VALUE	WRITE	READ
000h	Do not create any errors	No errors left to be inserted
001h	Create a single error	One error left to be inserted
002h	Create two errors	Two errors left to be inserted
3FFh	Create 1023 errors	1023 errors left to be inserted

Register Name: **NOE1**
Register Description: **Number Of Errors 1**
Register Address: **ECh**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Number of Errors Counter Bits 0 to 7 (C0 to C7). Bit C0 is the LSB of the 10-bit counter.

Register Name: **NOE2**
Register Description: **Number Of Errors 2**
Register Address: **EDh**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	C9	C8
Default	0	0	0	0	0	0	0	0

Bits 0 to 1/Number of Errors Counter Bits 8 to 9 (C8 to C9). Bit C9 is the MSB of the 10-bit counter.

26.1.1 Number Of Errors Left Register

The host can read the NOELx registers at any time to determine how many errors are left to be inserted.

Register Name: **NOEL1**
Register Description: **Number Of Errors Left 1**
Register Address: **EEh**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Number of Errors Left Counter Bits 0 to 7 (C0 to C7). Bit C0 is the LSB of the 10-bit counter.

Register Name: **NOEL2**
Register Description: **Number Of Errors Left 2**
Register Address: **EFh**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	C9	C8
Default	0	0	0	0	0	0	0	0

Bits 0 to 1/Number of Errors Left Counter Bits 8 to 9 (C8 to C9). Bit C9 is the MSB of the 10-bit counter.

27. INTERLEAVED PCM BUS OPERATION

In many architectures, the PCM outputs of individual framers are combined into higher speed PCM buses to simplify transport across the system backplane. The DS21Q55 can be configured to allow PCM data to be multiplexed into higher speed buses eliminating external hardware, saving board space and cost. The DS21Q55 can be configured for channel or frame interleave.

The interleaved PCM bus option (IBO) supports three bus speeds. The 4.096MHz bus speed allows two PCM data streams to share a common bus. The 8.192MHz bus speed allows four PCM data streams to share a common bus. The 16.384MHz bus speed allows eight PCM data streams to share a common bus. See Figure 30-1 for an example of four transceivers sharing a common 8.192MHz PCM bus. The receive elastic stores of each transceiver must be enabled. Via the IBO register the user can configure each transceiver for a specific bus position. For all IBO bus configurations each transceiver is assigned an exclusive position in the high-speed PCM bus. The 8kHz frame sync can be generated from the system backplane or from the first device on the bus. All other devices on the bus must have their frame syncs configured as inputs. Relative to this common frame sync, the devices will await their turn to drive or sample the bus according to the settings of the DA0, DA1, and DA2 bits of the IBOC register.

27.1 Channel Interleave Mode

In channel interleave mode, data is output to the PCM data-out bus one channel at a time from each of the connected devices until all channels of frame n from each device has been placed on the bus. This mode can be used even when the DS21Q55s are operating asynchronous to each other. The elastic stores will manage slip conditions.

27.2 Frame Interleave Mode

In frame interleave mode, data is output to the PCM data-out bus one frame at a time from each of the devices. This mode is used only when all connected devices are operating in a synchronous fashion (all inbound T1 or E1 lines are synchronous) and are synchronous with the system clock (system clock derived from T1 or E1 line). In this mode, slip conditions are not allowed.

Register Name: **IBOC**
Register Description: **Interleave Bus Operation Control Register**
Register Address: **C5h**

Bit #	7	6	5	4	3	2	1	0
Name	-	IBS1	IBS0	IBOSEL	IBOEN	DA2	DA1	DA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2/Device Assignment bits (DA0 to DA2).

DA2	DA1	DA0	DEVICE POSITION
0	0	0	1st Device on bus
0	0	1	2nd Device on bus
0	1	0	3rd Device on bus
0	1	1	4th Device on bus
1	0	0	5th Device on bus
1	0	1	6th Device on bus
1	1	0	7th Device on bus
1	1	1	8th Device on bus

Bit 3/Interleave Bus Operation Enable (IBOEN).
0 = Interleave Bus Operation disabled
1 = Interleave Bus Operation enabled

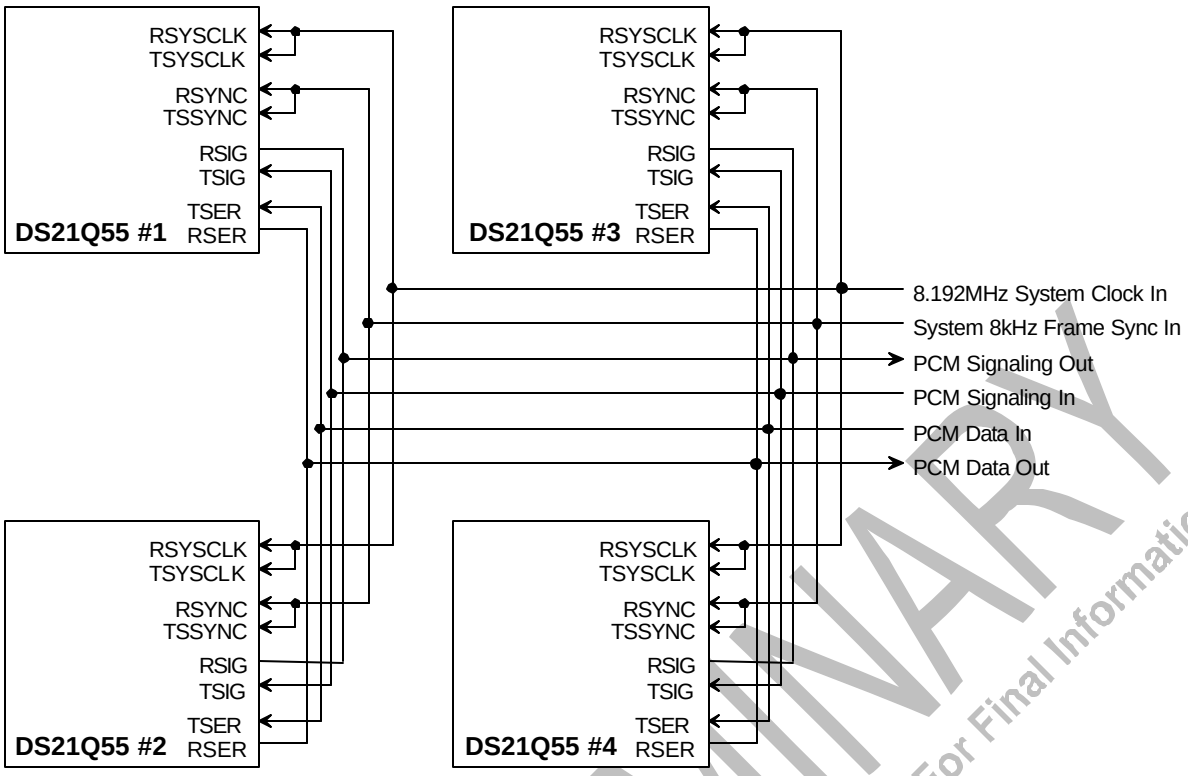
Bit 4/Interleave Bus Operation Select (IBOSEL). This bit selects channel- or frame-interleave mode.
0 = Channel Interleave
1 = Frame Interleave

Bits 5 to 6/IBO Bus Size bit 1 (IBS0 to IBS1). Indicates how many devices on the bus.

IBS1	IBS0	BUS SIZE
0	0	Two Devices on Bus
0	1	Four Devices on Bus
1	0	Eight Devices on Bus
1	1	Reserved for Future Use

Bit 7/Unused, must be set to zero for proper operation.

IBO EXAMPLE Figure 29-1

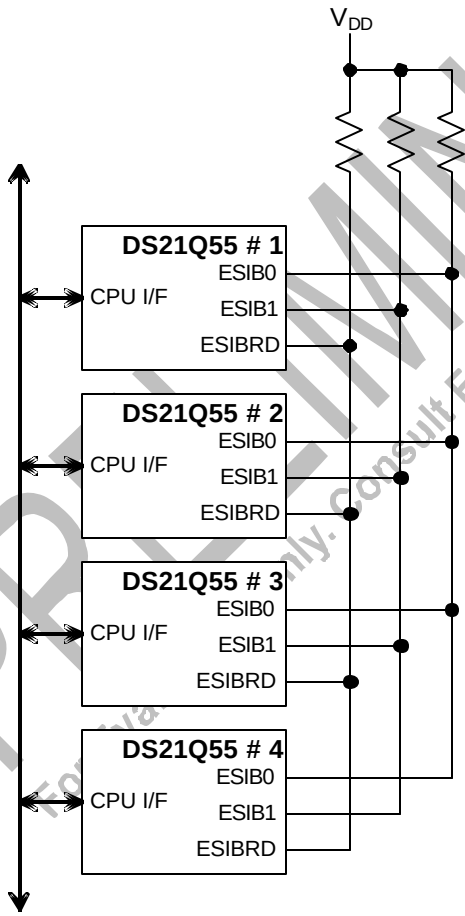


28. EXTENDED SYSTEM INFORMATION BUS (ESIB)

The ESIB allows two DS21Q55s to share an 8-bit CPU bus for the purpose of reporting alarms and interrupt status as a group. With a single bus read, the host can be updated with alarm or interrupt status from all members of the group. There are two control registers, ESIBCR1 and ESIBCR2, and four information registers, ESIB1, ESIB2, ESIB3, and ESIB4. As an example, eight DS21Q55s can be grouped into an ESIB group. A single read of the ESIB1 register of ANY member of the group will yield the interrupt status of all eight DS21Q55s. Therefore the host can determine which device or devices are causing an interrupt without polling all eight devices. Via ESIB2 the host can gather synchronization status on all members of the group. ESIB3 and ESIB4 can be programmed to report various alarms on a device by device basis.

There are three device pins involved in forming a ESIB group. These are ESIBS0, ESIBS1, and ESIBRD. A 10k pullup resistor must be provided on ESIBS0, ESIBS1, and ESIBRD.

ESIB GROUP OF FOUR DS21Q55s Figure 30-1



Register Name: **ESIBCR1**
Register Description: **Extended System Information Bus Control Register 1**
Register Address: **B0h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	ESIBSEL2	ESIBSEL1	ESIBSEL0	ESIEN
Default	0	0	0	0	0	0	0	0

Bit 0/Extended System Information Bus Enable (ESIEN).
0 = disabled
1 = enabled

Bits 1 to 3/Output Data Bus Line Select (ESIBSEL0 to ESIBSEL2). These bits tell the device which data bus bit to output the ESIB data on when one of the ESIB information registers is accessed. Each member of the ESIB group must have a unique bit selected.

ESIBSEL2	ESIBSEL1	ESIBSEL0	BUS BIT DRIVEN
0	0	0	AD0
0	0	1	AD1
0	1	0	AD2
0	1	1	AD3
1	0	0	AD4
1	0	1	AD5
1	1	0	AD6
1	1	1	AD7

Bit 4/Unused, must be set to zero for proper operation.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **ESIBCR2**
Register Description: **Extended System Information Bus Control Register 2**
Register Address: **B1h**

Bit #	7	6	5	4	3	2	1	0
Name	-	ESI4SEL2	ESI4SEL1	ESI4SEL0	-	ESI3SEL2	ESI3SEL1	ESI3SEL0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2/Address ESI3 Data Output Select (ESI3SEL0 to ESI3SEL2). These bits select what status is to be output when the device decodes an ESI3 address during a bus read operation.

ESI3SEL2	ESI3SEL1	ESI3SEL0	STATUS OUTPUT (T1 MODE)	STATUS OUTPUT (E1 MODE)
0	0	0	RBL	RUA1
0	0	1	RYEL	RRA
0	1	0	LUP	RDMA
0	1	1	LDN	V52LNK
1	0	0	SIGCHG	SIGCHG
1	0	1	ESSLIP	ESSLIP
1	1	0	-	-
1	1	1	-	-

Bit 3/Unused, must be set to zero for proper operation.

Bits 4 to 6/Address ESI4 Data Output Select (ESI4SEL0 to ESI4SEL2). These bits select what status is to be output when the device decodes an ESI4 address during a bus-read operation.

ESI4SEL2	ESI4SEL1	ESI4SEL0	STATUS OUTPUT (T1 MODE)	STATUS OUTPUT (E1 MODE)
0	0	0	RBL	RUA1
0	0	1	RYEL	RRA
0	1	0	LUP	RDMA
0	1	1	LDN	V52LNK
1	0	0	SIGCHG	SIGCHG
1	0	1	ESSLIP	ESSLIP
1	1	0	-	-
1	1	1	-	-

Bit 7/Unused, must be set to zero for proper operation.

Register Name: **ESIB1**
Register Description: **Extended System Information Bus Register 1**
Register Address: **B2h**

Bit #	7	6	5	4	3	2	1	0
Name	DISn	DISn	DISn	DISn	DISn	DISn	DISn	DISn
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Device Interrupt Status (DISn). Causes all devices participating in the ESIB group to output their interrupt status on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR1 register.

Register Name: **ESIB2**
Register Description: **Extended System Information Bus Register 2**
Register Address: **B3h**

Bit #	7	6	5	4	3	2	1	0
Name	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Device Receive Loss of Sync (DRLOSn). Causes all devices participating in the ESIB group to output their frame synchronization status on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR1 register.

Register Name: **ESIB3**
Register Description: **Extended System Information Bus Register 3**
Register Address: **B4h**

Bit #	7	6	5	4	3	2	1	0
Name	UST1n	UST1n	UST1n	UST1n	UST1n	UST1n	UST1n	UST1n
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/User-Selected Status 1 (UST1n). Causes all devices participating in the ESIB group to output status or alarms as selected by the ESI3SEL0 to ESI3SEL2 bits in the ESIBCR2 configuration register on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR2 register.

Register Name: **ESIB4**
Register Description: **Extended System Information Bus Register 4**
Register Address: **B5h**

Bit #	7	6	5	4	3	2	1	0
Name	UST2n	UST2n	UST2n	UST2n	UST2n	UST2n	UST2n	UST2n
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/User-Selected Status 2 (UST2n). Causes all devices participating in the ESIB group to output status or alarms as selected by the ESI4SEL0 to ESI4SEL2 bits in the ESIBCR2 configuration register on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR2 register.

29. PROGRAMMABLE BACKPLANE CLOCK SYNTHESIZER

The DS21Q55 contains an on-chip clock synthesizer that generates a user-selectable clock referenced to the recovered receive clock (RCLK). The synthesizer uses a phase-locked loop to generate low-jitter clocks. Common applications include generation of port and back plane system clocks.

Register Name: **CCR2**
Register Description: **Common Control Register 2**
Register Address: **71h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	BPCS1	BPCS0	BPEN
Default	0	0	0	0	0	0	0	0

Bit 0/Back Plane Clock Enable (BPEN).
0 = disable BPCLK pin (Pin held at logic 0)
1 = enable BPCLK pin

Bits 1 to 2/Back Plane Clock Selects (BPCS0, BPCS1).

BPCS1	BPCS0	BPCLK FREQUENCY (MHz)
0	0	16.384
0	1	8.192
1	0	4.096
1	1	2.048

Bit 3/Unused, must be set to zero for proper operation.

Bit 4/Unused, must be set to zero for proper operation.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

30. FRACTIONAL T1/E1 SUPPORT

The DS21Q55 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in fractional T1/E1 or ISDN-PRI applications. This is accomplished by assigning an alternate function to the RCHCLK and TCHCLK pins. When the gapped clock feature is enabled, a gated clock is output on the RCHCLK and/or TCHCLK pins. The channel selection is controlled via the special per-channel control registers. No clock is generated at the F-bit position. The receive and transmit paths have independent enables. Channel formats supported include 56kbps and 64kbps.

When 56kbps mode is selected, the clock corresponding to the data/control bit in the channel is omitted. Only the seven most significant bits of the channel have clocks.

Register Name: **CCR3**
Register Description: **Common Control Register 3**
Register Address: **72h**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	TDATFMT	TGPCKEN	RDATFMT	RGPCKEN
Default	0	0	0	0	0	0	0	0

Bit 0/Receive Gapped-Clock Enable (RGPCKEN).
0 = RCHCLK functions normally
1 = enable gapped-bit clock output on RCHCLK

Bit 1/Receive Channel-Data Format (RDATFMT).
0 = 64kbps (data contained in all 8 bits)
1 = 56kbps (data contained in 7 out of the 8 bits)

Bit 2/Transmit Gapped-Clock Enable (TGPCKEN).
0 = TCHCLK functions normally
1 = enable gapped-bit clock output on TCHCLK

Bit 3/Transmit Channel-Data Format (TDATFMT).
0 = 64kbps (data contained in all 8 bits)
1 = 56kbps (data contained in 7 out of the 8 bits)

Bit 4/Unused, must be set to zero for proper operation.

Bit 5/Unused, must be set to zero for proper operation.

Bit 6/Unused, must be set to zero for proper operation.

Bit 7/Unused, must be set to zero for proper operation.

31. JTAG-BOUNDARY-SCAN ARCHITECTURE AND TEST-ACCESS PORT

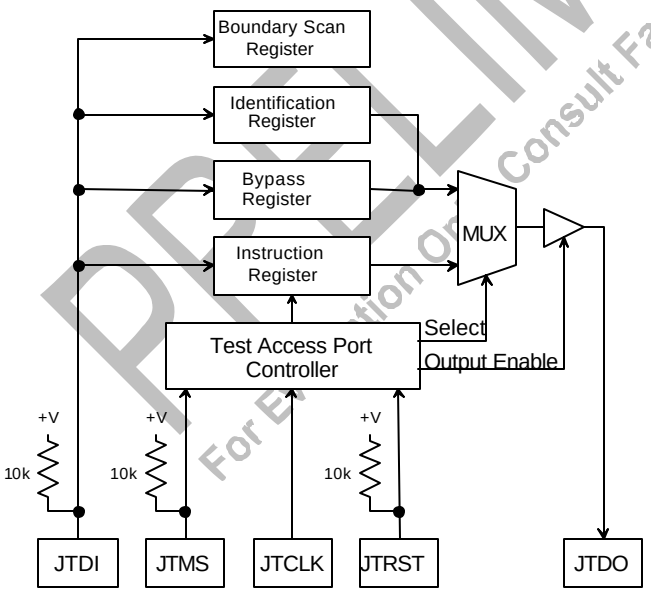
The DS21Q55 is an MCM consisting of 4 DS2155s. Each device has its on JTAG state machine and therefore is treated as 4 separate devices when testing. The following description refers to the DS2155 JTAG function.

The DS2155 IEEE 1149.1 design supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGH-Z, CLAMP, and IDCODE (Figure 21). The DS21Q55 contains the following as required by IEEE 1149.1 Standard Test-Access Port and Boundary-Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The Test Access Port has the necessary interface pins: JTRST, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details.

JTAG FUNCTIONAL BLOCK DIAGRAM Figure 34-1



TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK (Figure 34-2).

Test-Logic-Reset

Upon power-up, the TAP controller will be in the test-logic-reset state. The instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

Run-Test-Idle

The run-test-idle is used between scan operations or during specific tests. The instruction register and test registers will remain idle.

Select-DR-Scan

All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the select-IR-scan state.

Capture-DR

Data can be parallel-loaded into the test-data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the shift-DR state if JTMS is LOW or it will go to the exit1-DR state if JTMS is HIGH.

Shift-DR

The test-data register selected by the current instruction will be connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

Exit1-DR

While in this state, a rising edge on JTCLK will put the controller in the update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW will put the controller in the pause-DR state.

Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH will put the controller in the exit2-DR state.

Exit2-DR

A rising edge on JTCLK with JTMS HIGH while in this state will put the controller in the update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS LOW will enter the shift-DR state.

Update-DR

A falling edge on JTCLK while in the update-DR state will latch the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

Select-IR-Scan

All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the capture-IR state and will initiate a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the test-logic-reset state.

Capture-IR

The capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller will enter the shift-IR state.

Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register as well as all test registers remain at their previous states. A rising edge on JTCLK with JTMS HIGH will move the controller to the exit1-IR state. A rising edge on JTCLK with JTMS LOW will keep the controller in the shift-IR state while moving data one stage thorough the instruction shift register.

Exit1-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the update-IR state and terminate the scanning process.

Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK will put the controller in the exit2-IR state. The controller will remain in the pause-IR state if JTMS is LOW during a rising edge on JTCLK.

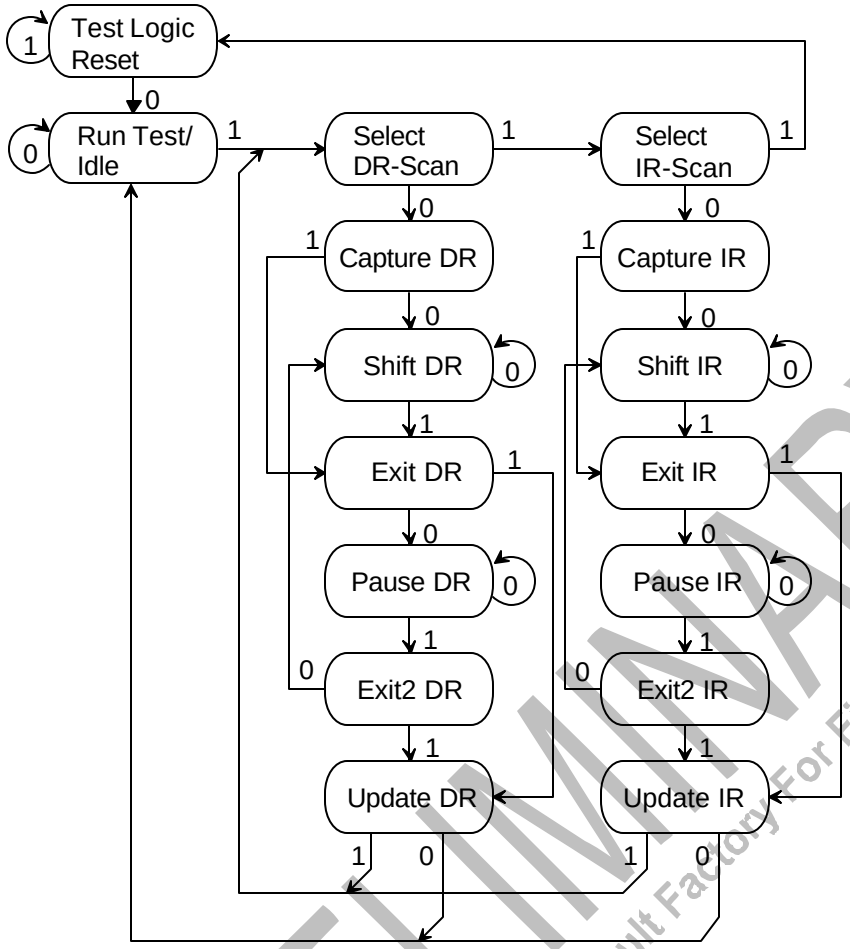
Exit2-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the update-IR state. The controller will loop back to shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS LOW, will put the controller in the run-test-idle state. With JTMS HIGH, the controller will enter the select-DR-scan state.

TAP CONTROLLER STATE DIAGRAM Figure 34-2



31.1 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the shift-IR state, the instruction shift register will be connected between JTDI and JTDO. While in the shift-IR state, a rising edge on JTCLK with JTMS LOW will shift the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the exit1-IR state or the exit2-IR state with JTMS HIGH will move the controller to the update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS2155 and its respective operational binary codes are shown in Table 34-1.

INSTRUCTION CODES FOR IEEE 1149.1 ARCHITECTURE Table 34-1

INSTRUCTION	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGH-Z	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification that supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the shift-DR state.

BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The boundary scan register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

HIGH-Z

All digital outputs of the device will be placed in a high impedance state. The BYPASS register will be connected between JTDI and JTDO.

IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code will be loaded into the identification register on the rising edge of JTCLK following entry into the capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During test-logic-reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version (Table 34-2). Table 34-3 lists the device ID codes for the devices.

ID CODE STRUCTURE Table 34-2

MSB			LSB
Version Contact Factory	Device ID	JEDEC	1
4 bits	16 bits	00010100001	1

DEVICE ID CODES Table 34-3

DEVICE	16-BIT ID
DS2155	0010h
DS21354	0005h
DS21554	0003h
DS21352	0004h

DS21552	0002h

31.2 Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included with the DS2155 design. This test register is the identification register and is used with the IDCODE instruction and the test-logic-reset state of the TAP controller.

31.3 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is n bits in length. See Table 34-4 for all of the cell bit locations and definitions.

31.4 Bypass Register

This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGH-Z instructions that provides a short path between JTDI and JTDO.

31.5 Identification Register

The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the test-logic-reset state. See Tables 34-2 and 34-3 for more information about bit usage.

BOUNDARY SCAN CONTROL BITS Table 34-4

NXA = Not Externally Available

BIT	PIN	SYMBOL	TYPE	CONTROL BIT DESCRIPTION
2	1	RCHBLK	O	
	2	JTMS	I	
1	3	BPCLK	O	
	4	JTCLK	I	
	5	JTRST	I	
0	6	RCL **(NXA)**	O	
	7	JTDI	I	
77	8	UOP0 **(NXA)**	O	
76	9	UOP1 **(NXA)**	O	
	10	JTDO	O	
75	11	BTS	I	
74	12	LIUC	I	
73	13	8XCLK **(NXA)**	O	
72	14	TSTRST	I	
71	15	UOP2 **(NXA)**	O	
	16	RTIP	I	
	17	RRING	I	
	18	RV_{DD}	–	
	19	RV_{SS}	–	
	20	RV_{SS}	–	
	21	MCLK	I	
	22	XTALD **(NXA)**	O	
70	23	UOP3 **(NXA)**	O	
	24	RV_{SS}	–	
69	25	INT	O	
	26	N/C	–	
	27	N/C	–	
	28	N/C	–	
	29	TTIP	O	
	30	TV_{SS}	–	
	31	TV_{DD}	–	
	32	TRING	O	
68	33	TCHBLK	O	
67	34	TLCLK	O	
66	35	TLINK	I	
65	-	ESIBS0.cntl	-	0 = ESIBS0 is an input; 1 = ESIBS0 is an output
64	36	ESIBS0	I/O	
63	–	TSYNC.cntl	–	0 = TSYNC is an input; 1 = TSYNC is an output
62	37	TSYNC	I/O	
61	38	TPOSI	I	
60	39	TNEGI	I	
59	40	TCLKI	I	
58	41	TCLKO	O	
57	42	TNEGO	O	
56	43	TPOSO	O	
	44	DV_{DD}	–	
	45	DV_{SS}	–	
55	46	TCLK	I	
54	47	TSER	I	

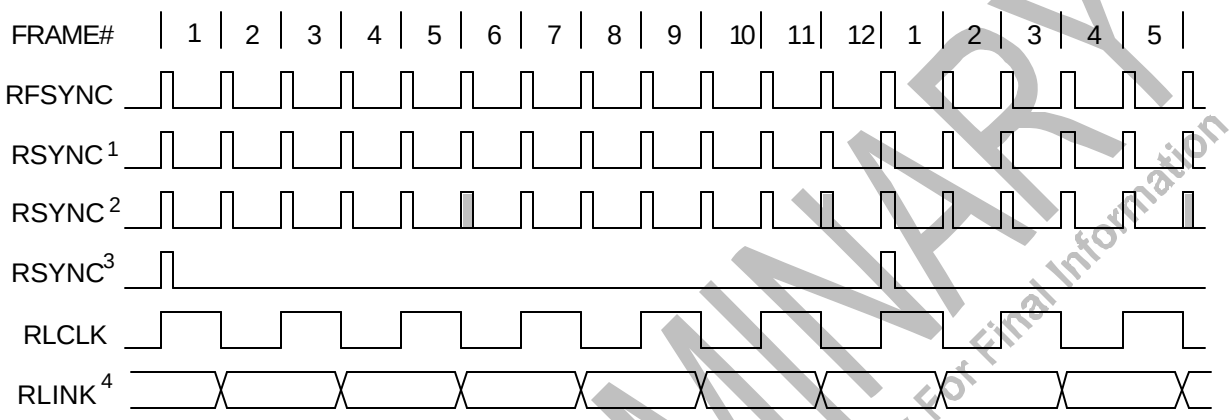
BIT	PIN	SYMBOL	TYPE	CONTROL BIT DESCRIPTION
53	48	TSIG	I	
52	49	TESO **(NXA)**	O	
51	50	TDATA **(NXA)**	I	
50	51	TSYSCLK	I	
49	52	TSSYNC	I	
48	53	TCHCLK	O	
47	-	ESIBS1.cntl	-	0 = ESIBS1 is an input; 1 = ESIBS1 is an output
46	54	ESIBS1	I/O	
45	55	MUX	I	
44	–	BUS.cntl	–	0 = D0-D7/AD0-AD7 are inputs; 1 = D0–D7/AD0–AD7 are outputs
43	56	D0/AD0	I/O	
42	57	D1/AD1	I/O	
41	58	D2/AD2	I/O	
40	59	D3/AD3	I/O	
	60	DV_{SS}	–	
	61	DV_{DD}	–	
39	62	D4/AD4	I/O	
38	63	D5/AD5	I/O	
37	64	D6/AD6	I/O	
36	65	D7/AD7	I/O	
35	66	A0	I	
34	67	A1	I	
33	68	A2	I	
32	69	A3	I	
31	70	A4	I	
30	71	A5	I	
29	72	A6	I	
28	73	A7/ALE(AS)	I	
27	74	RD*(DS*)	I	
26	75	CS*	I	
25	-	ESIBRD.cntl	-	0 = ESIBRD is an input;1 = ESIBRD is an output
24	76	ESIBRD	I/O	
23	77	WR*(R/W*)	I	
22	78	RLINK	O	
21	79	RLCLK	O	
	80	DV_{SS}	–	
	81	DV_{DD}		
20	82	RCLK	O	
	83	DV_{DD}	–	
	84	DV_{SS}	–	
19	85	RDATA **(NXA)**	O	
18	86	RPOSI	I	
17	87	RNEGI	I	
16	88	RCLKI	I	
15	89	RCLKO	O	
14	90	RNEGO	O	
13	91	RPOSO	O	
12	92	RCHCLK	O	
11	93	RSIGF	O	
10	94	RSIG	O	
9	95	RSER	O	
8	96	RMSYNC	O	

BIT	PIN	SYMBOL	TYPE	CONTROL BIT DESCRIPTION
7	97	RFSYNC	O	
6	–	RSYNC.cntl	–	0 = RSYNC is an input; 1 = RSYNC is an output
5	98	RSYNC	I/O	
4	99	RLOS/LOTC	O	
3	100	RSYSCLK	I	

32. FUNCTIONAL TIMING DIAGRAMS

32.1 T1 Mode

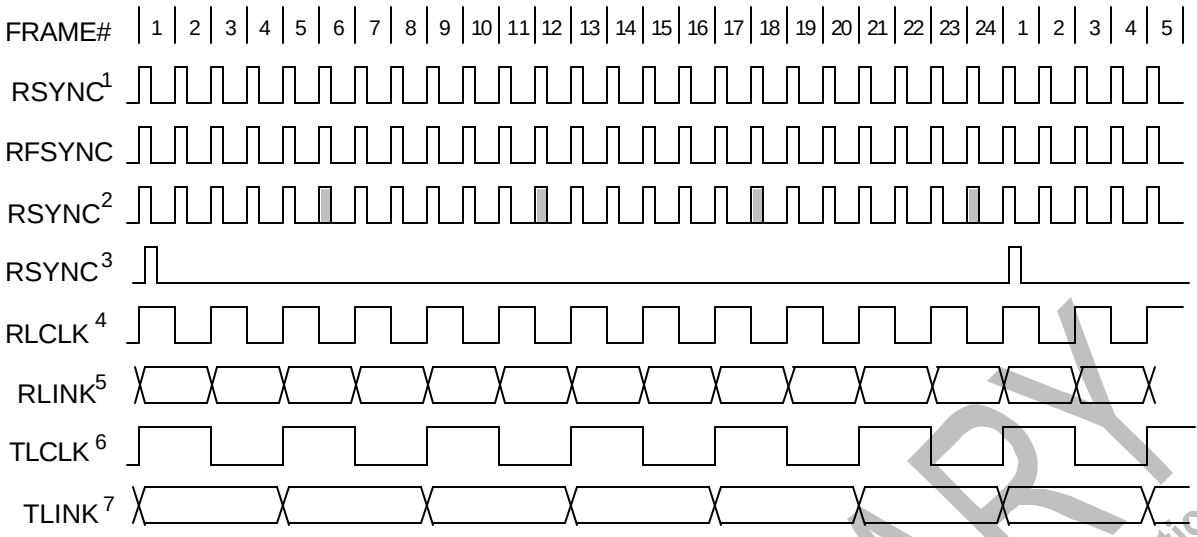
RECEIVE SIDE D4 TIMING Figure 35-1



NOTES:

1) RSYNC in the frame mode (IOCR1.5 = 0) and double-wide frame sync is not enabled (IOCR1.6 = 0).
2) RSYNC in the frame mode (IOCR1.5 = 0) and double-wide frame sync is enabled (IOCR1.6 = 1).
3) RSYNC in the multiframe mode (IOCR1.5 = 1).
4) RLINK data (Fs-bits) is updated one bit prior to even frames and held for two frames.

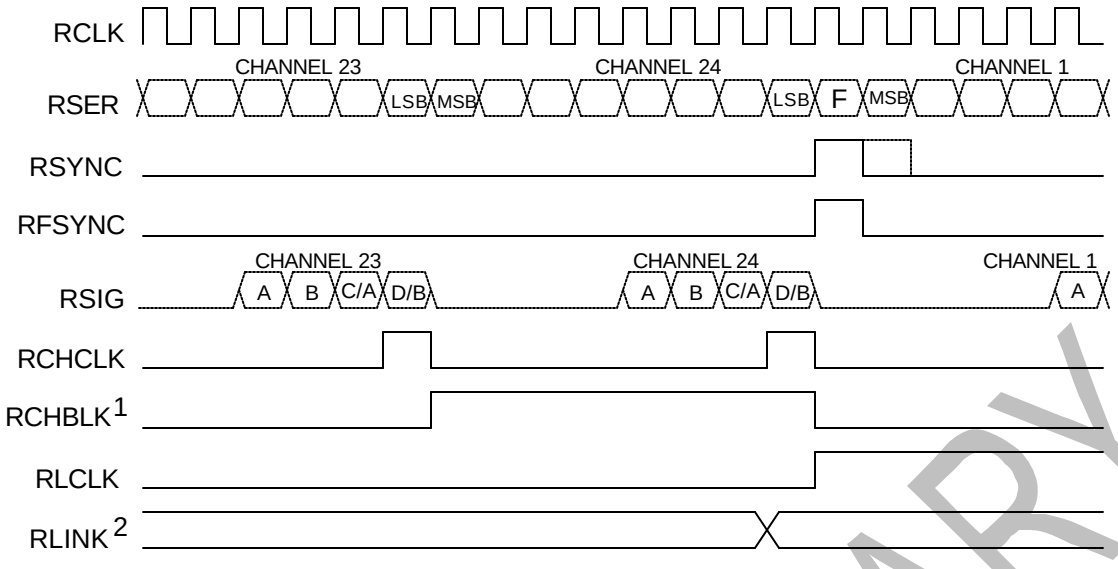
RECEIVE SIDE ESF TIMING Figure 35-2



NOTES:

1) RSYNC in frame mode (IOCR1.4 = 0) and double wide frame sync is not enabled (IOCR1.6 = 0).
2) RSYNC in frame mode (IOCR1.4 = 0) and double wide frame sync is enabled (IOCR1.6 = 1).
3) RSYNC in multiframe mode (IOCR1.4 = 1).
4) ZBTSI mode disabled (T1RCR2.2 = 0).
5) RLINK data (FDL bits) is updated one bit time before odd frames and held for two frames.
6) ZBTSI mode is enabled (T1RCR2.2 = 1).
7) RLINK data (Z bits) is updated one bit time before odd frames and held for four frames.

RECEIVE SIDE BOUNDARY TIMING (With Elastic Store Disabled) Figure 35-3

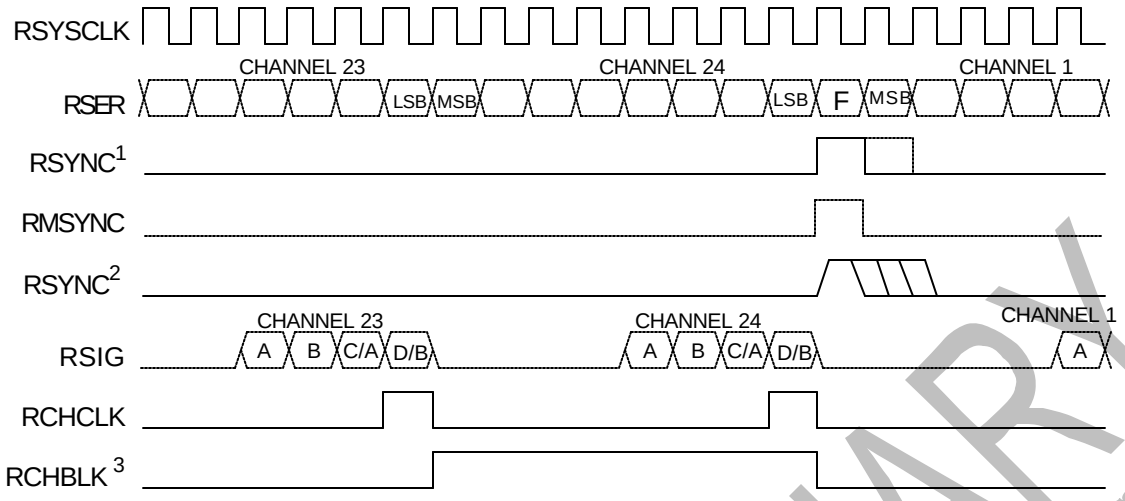


NOTES:

1) RCHBLK is programmed to block channel 24.
2) Shown is RLINK/RLCLK in the ESF framing mode.

RECEIVE SIDE 1.544MHz BOUNDARY TIMING (With Elastic Store Enabled)

Figure 35-4

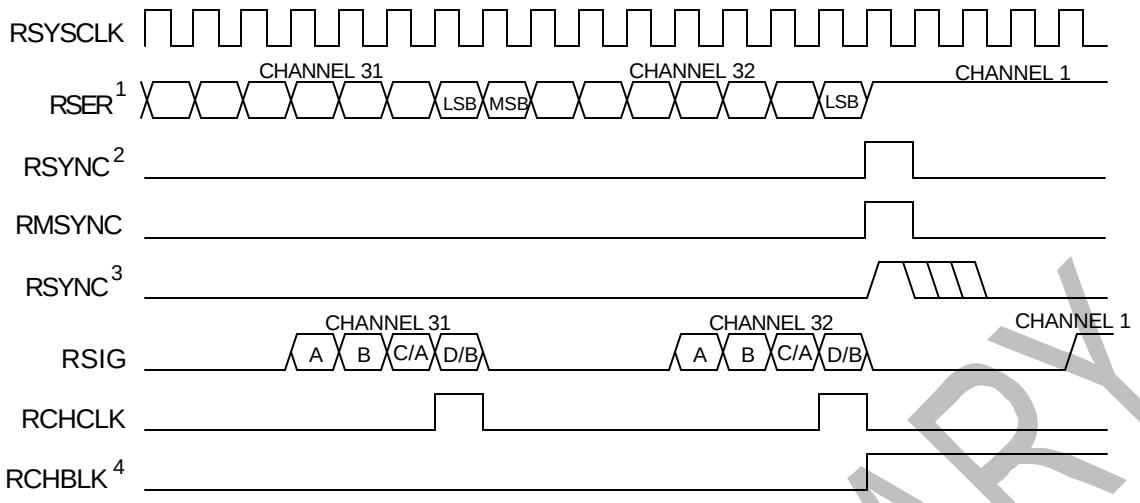


NOTES:

1) RSYNC is in the output mode (IOCR1.4 = 0).
2) RSYNC is in the input mode (IOCR1.4 = 1).
3) RCHBLK is programmed to block channel 24.

RECEIVE SIDE 2.048MHz BOUNDARY TIMING (With Elastic Store Enabled)

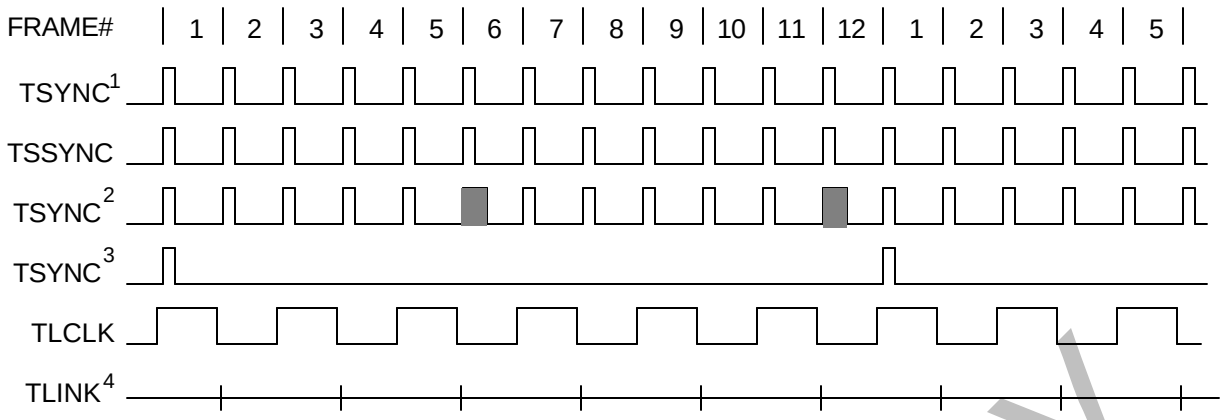
Figure 35-5



NOTES:

1) RSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 are forced to one.
2) RSYNC is in the output mode (IOCR1.4 = 0).
3) RSYNC is in the input mode (IOCR1.4 = 1).
4) RCHBLK is forced to one in the same channels as RSER (Note 1).
5) The F-bit position is passed through the receive-side elastic store.

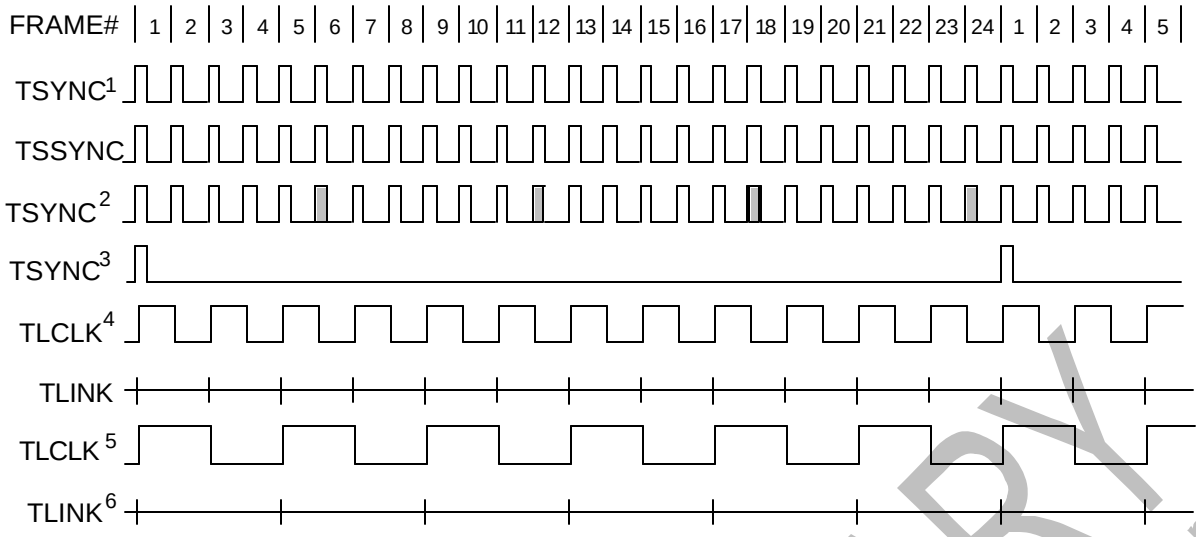
TRANSMIT SIDE D4 TIMING Figure 35-6



NOTES:

1) TSYNC in the frame mode (IOCR1.2 = 0) and double-wide frame sync is not enabled (IOCR1.1 = 0).
2) TSYNC in the frame mode (IOCR1.2 = 0) and double-wide frame sync is enabled (IOCR1.1 = 1).
3) TSYNC in the multiframe mode (IOCR1.2 = 1).
4) TLINK data (Fs-bits) is sampled during the F-bit position of even frames for insertion into the outgoing T1 stream when enabled via T1TCR1.2.

TRANSMIT SIDE ESF TIMING Figure 35-7

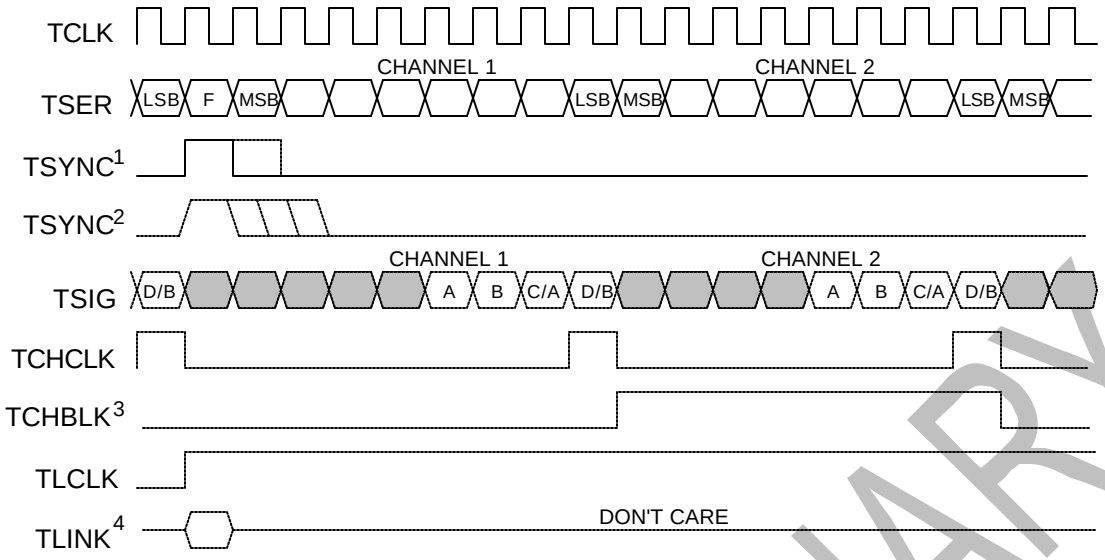


NOTES:

1) TSYNC in frame mode (IOCR1.2 = 0) and double-wide frame sync is not enabled (IOCR1.3 = 0).
2) TSYNC in frame mode (IOCR1.2 = 0) and double-wide frame sync is enabled (IOCR1.3 = 1).
3) TSYNC in multiframe mode (IOCR1.2 = 1).
4) TLINK data (FDL bits) sampled during the F-bit time of odd frame and inserted into the outgoing T1 stream if enabled via TCR1.2.
5) ZBTSI mode is enabled (T1TCR2.1 = 1).
6) TLINK data (Z bits) sampled during the F-bit time of frames 1, 5, 9, 13, 17, and 21 and inserted into the outgoing stream if enabled via T1TCR1.2.

TRANSMIT SIDE BOUNDARY TIMING (With Elastic Store Disabled)

Figure 35-8

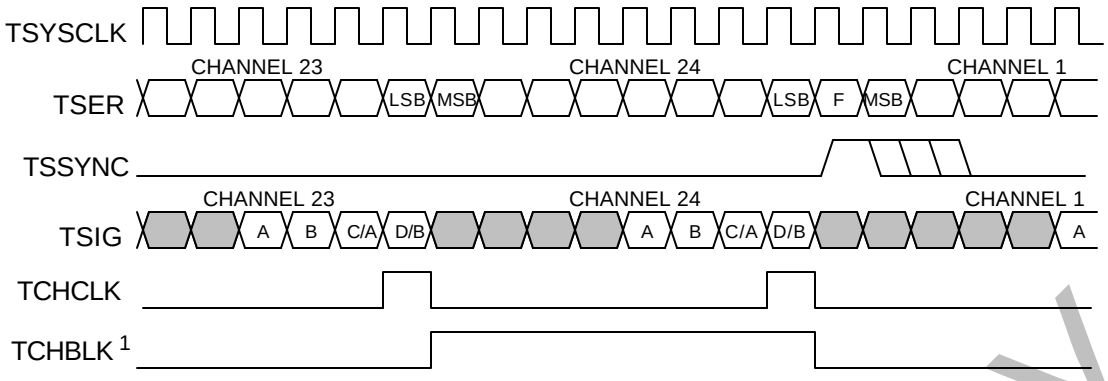


NOTES:

1) TSYNC is in the output mode (IOCR1.1 = 1).
2) TSYNC is in the input mode (IOCR1.1 = 0).
3) TCHBLK is programmed to block channel 2.
4) Shown is TLINK/TLCLK in the ESF framing mode.

TRANSMIT SIDE 1.544MHz BOUNDARY TIMING (With Elastic Store Enabled)

Figure 35-9

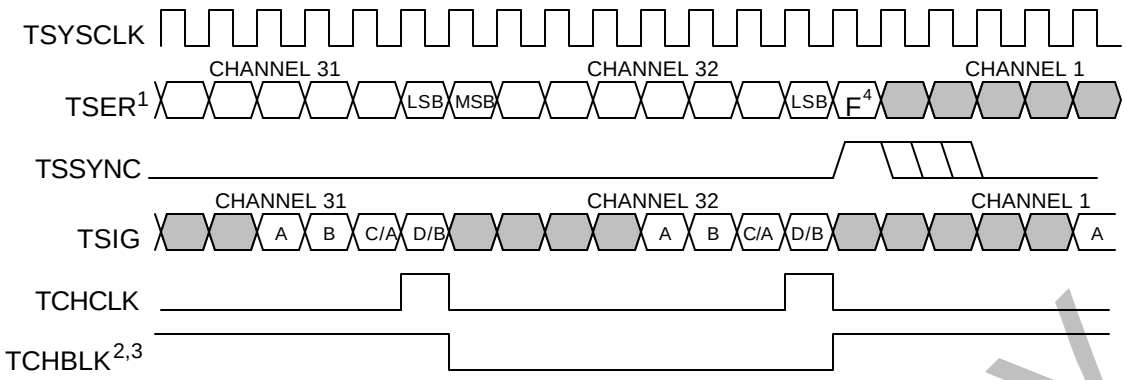


NOTE:

1) TCHBLK is programmed to block channel 24 (if the TPCSI bit is set, then the signaling data at TSIG will be ignored during channel 24).

TRANSMIT SIDE 2.048MHz BOUNDARY TIMING (With Elastic Store Enabled)

Figure 35-11

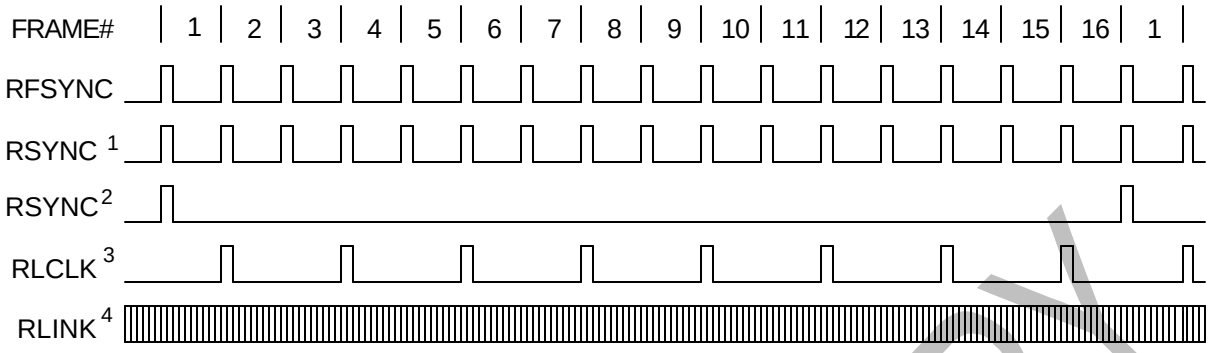


NOTES:

1) TSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 is ignored.
2) TCHBLK is programmed to block channel 31 (if the TPCSI bit is set, then the signaling data at TSIG will be ignored).
3) TCHBLK is forced to one in the same channels as TSER is ignored (Note 1).
4) The F-bit position for the T1 frame is sampled and passed through the transmit side elastic store into the MSB bit position of channel 1. (Normally the transmit side formatter overwrites the F-bit position unless the formatter is programmed to pass-through the F-bit position).

32.2 E1 Mode

RECEIVE SIDE TIMING Figure 35-11

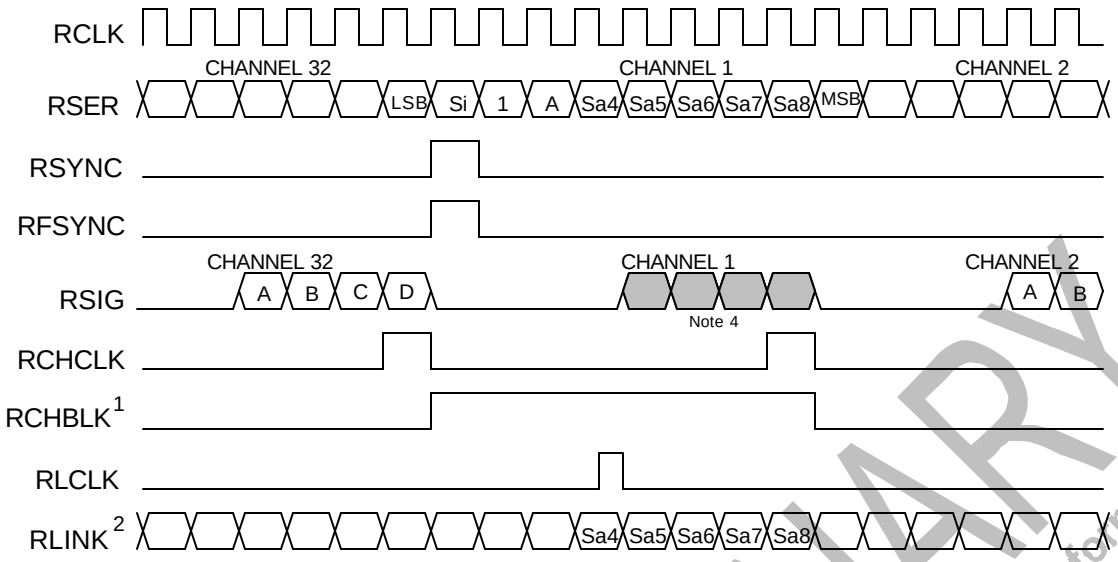


NOTES:

1) RSYNC in frame mode (IOCR1.5 = 0).
2) RSYNC in multiframe mode (IOCR1.5 = 1).
3) RLCLK is programmed to output just the Sa bits.
4) RLINK will always output all five Sa bits as well as the rest of the receive data stream.
5) This diagram assumes the CAS MF begins in the RAF frame.

RECEIVE SIDE BOUNDARY TIMING (With Elastic Store Disabled)

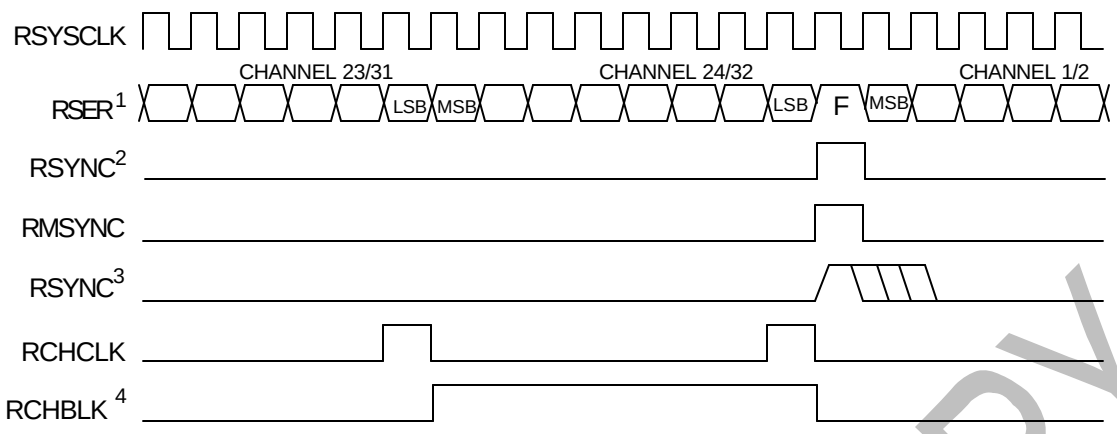
Figure 35-12



NOTES:

1) RCHBLK is programmed to block channel 1.
2) RLCLK is programmed to mark the Sa4 bit in RLINK.
3) Shown is a RNAF frame boundary.
4) RSIG normally contains the CAS multiframe-alignment nibble (0000) in channel 1.

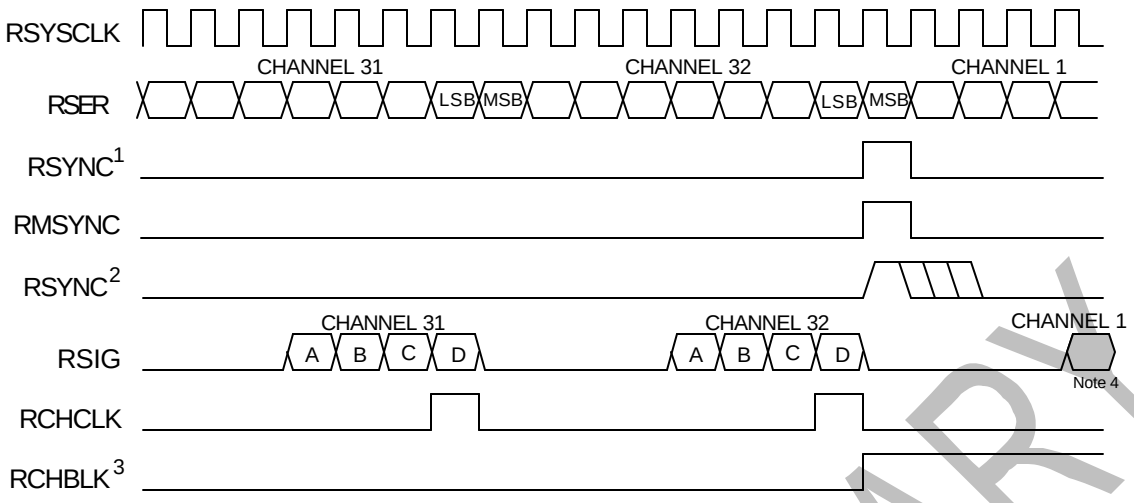
RECEIVE SIDE BOUNDARY TIMING, RSYSCLK = 1.544MHz (With Elastic Store Enabled) Figure 35-13



NOTES:

1) Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to one).
2) RSYNC in the output mode (IOCR1.4 = 0).
3) RSYNC in the input mode (IOCR1.4 = 1).
4) RCHBLK is programmed to block channel 24.

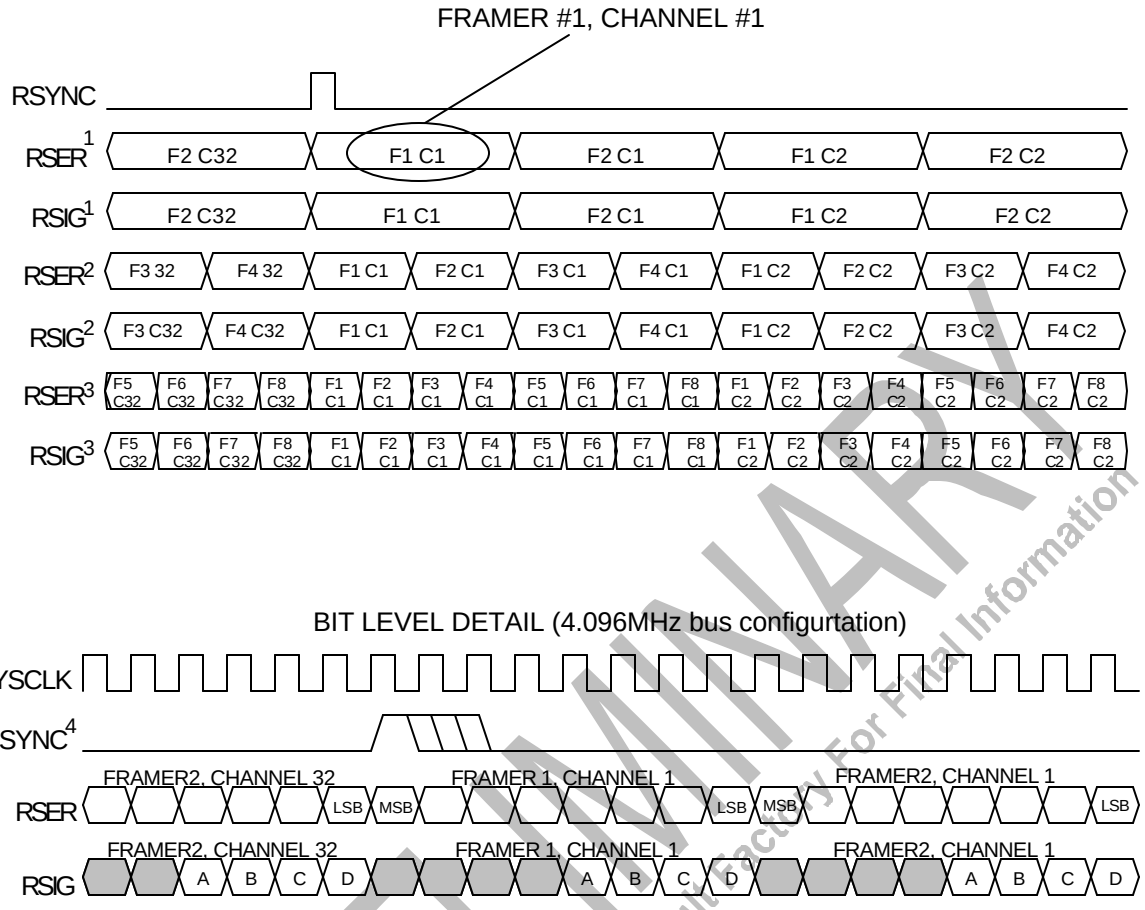
RECEIVE SIDE BOUNDARY TIMING, RSYSCLK = 2.048MHz (With Elastic Store Enabled) Figure 35-14



NOTES:

1) RSYNC is in the output mode (IOCR1.4 = 0).
2) RSYNC is in the input mode (IOCR1.4 = 1).
3) RCHBLK is programmed to block channel 1.
4) RSIG normally contains the CAS multiframe-alignment nibble (0000) in channel 1.

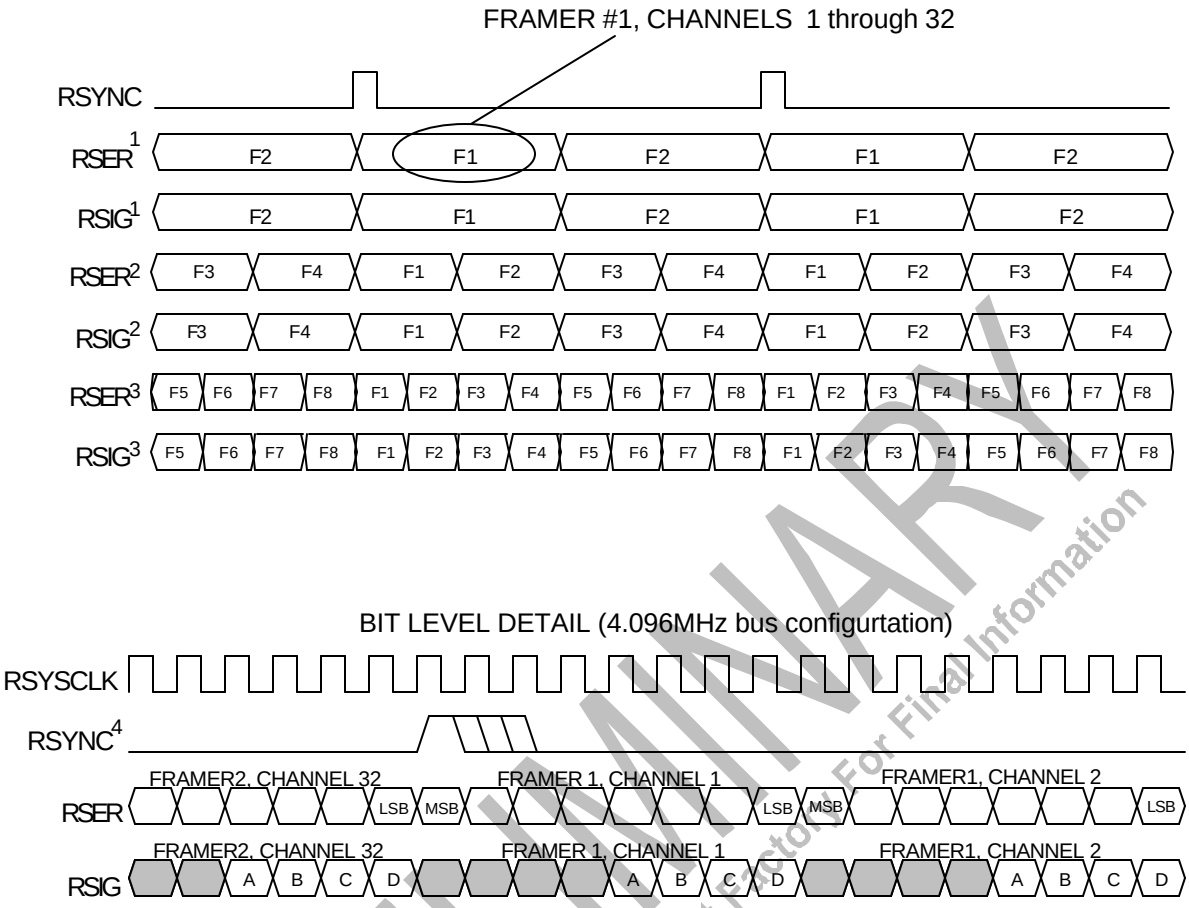
RECEIVE IBO CHANNEL INTERLEAVE MODE TIMING Figure 35-15



NOTES:

1) 4.096MHz bus configuration.
2) 8.192MHz bus configuration.
3) 16.384MHz bus configuration.
4) RSYNC is in the input mode (IOCR1.4 = 0).

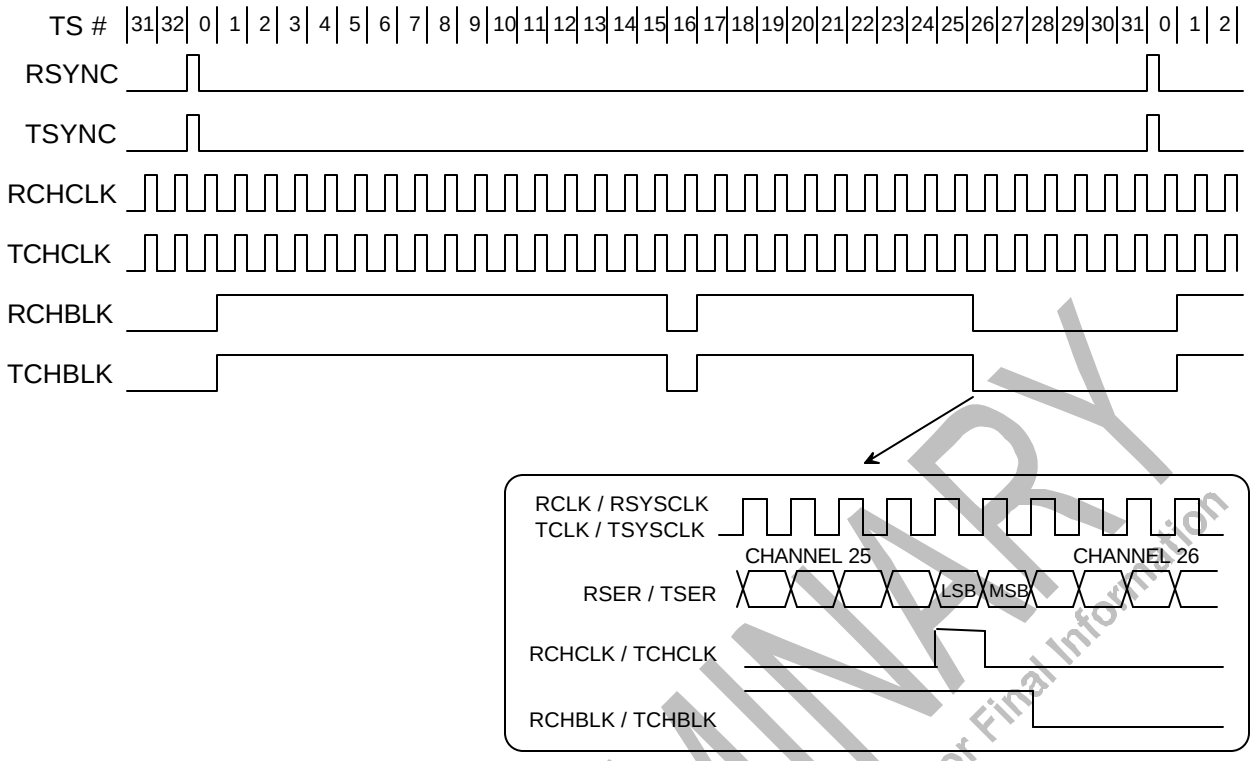
RECEIVE IBO FRAME INTERLEAVE MODE TIMING Figure 35-16



NOTES:

1) 4.096MHz bus configuration.
2) 8.192MHz bus configuration.
3) 16.384MHz bus configuration
4) RSYNC is in the input mode (IOCR1.4 = 0).

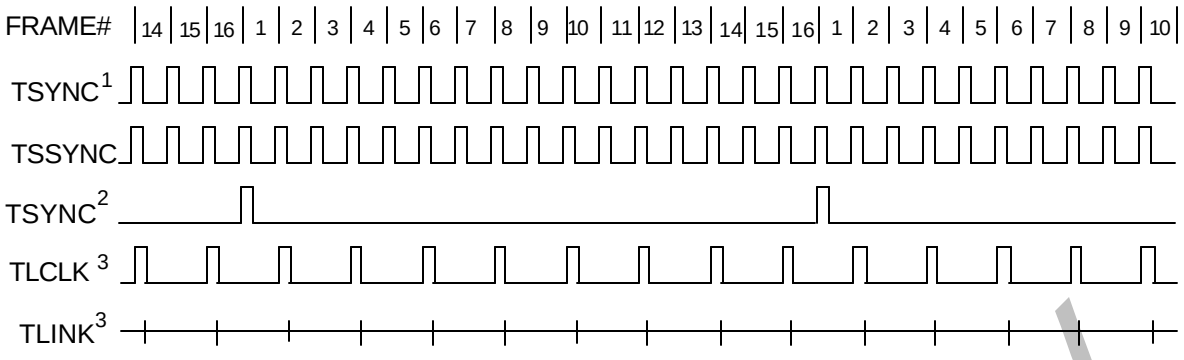
G.802 TIMING, E1 MODE ONLY Figure 35-17



NOTE:

1) RCHBLK or TCHBLK programmed to pulse high during timeslots 1 through 15, 17 through 25, and bit 1 of timeslot 26.

TRANSMIT SIDE TIMING Figure 35-18

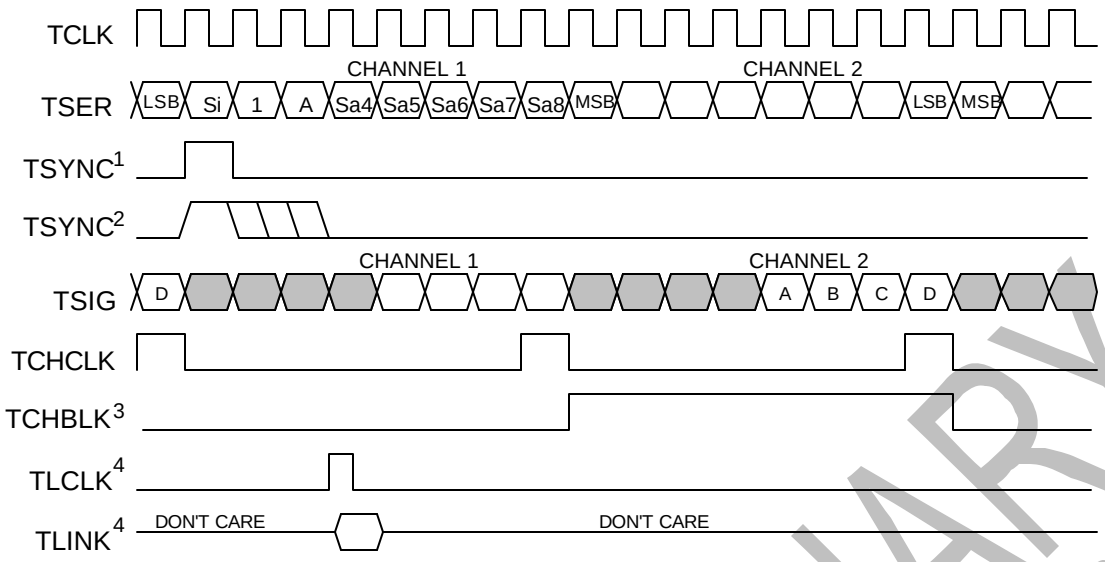


NOTES:

1) TSYNC in frame mode (IOCR1.2 = 0).
2) TSYNC in multiframe mode (IOCR1.2 = 1).
3) TLINK is programmed to source just the Sa4 bit.
4) This diagram assumes both the CAS MF and the CRC4 MF begin with the TAF frame.
5) TLINK and TLCLK are not synchronous with TSSYNC.

TRANSMIT SIDE BOUNDARY TIMING (With Elastic Store Disabled)

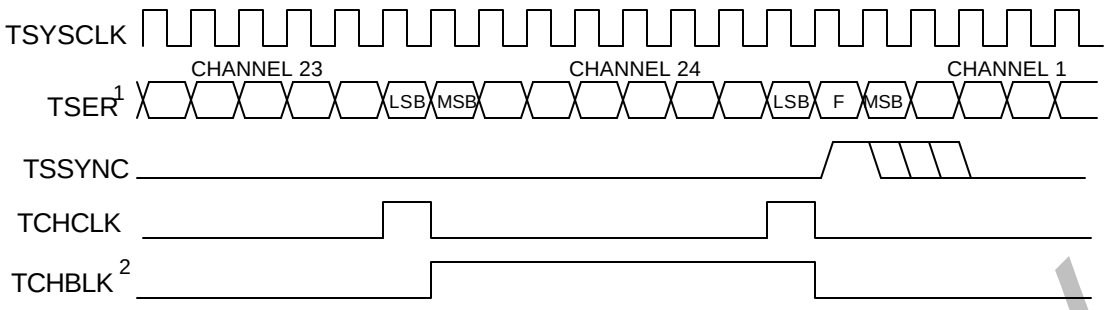
Figure 35-19



NOTES:

1) TSYNC is in the output mode (IOCR1.1 = 1.)
2) TSYNC is in the input mode (IOCR1.1 = 0).
3) TCHBLK is programmed to block channel 2.
4) TLINK is programmed to source the Sa4 bit.
5) The signaling data at TSIG during channel 1 is normally overwritten in the transmit formatter with the CAS multiframe-alignment nibble (0000).
6) Shown is a TNAF frame boundary.

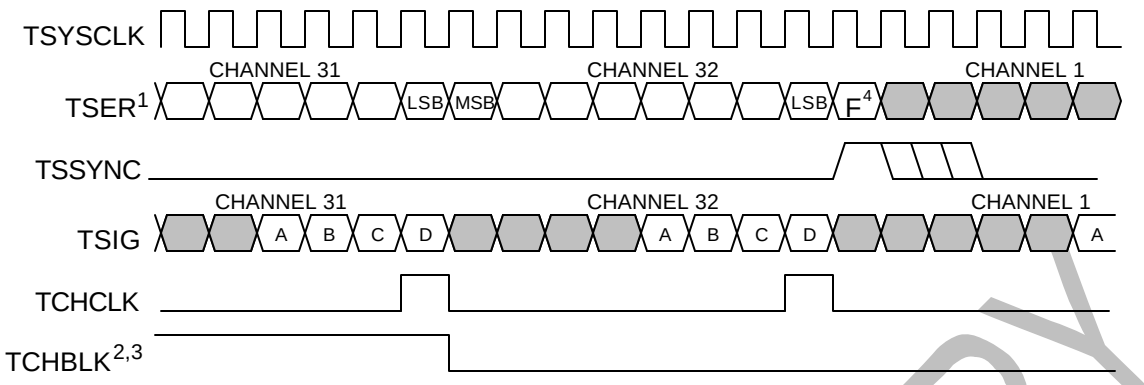
TRANSMIT SIDE BOUNDARY TIMING, TSYSCLK = 1.544MHz (With Elastic Store Enabled) Figure 35-20



NOTES:

1) The F-bit position in the TSER data is ignored.
2) TCHBLK is programmed to block channel 24.

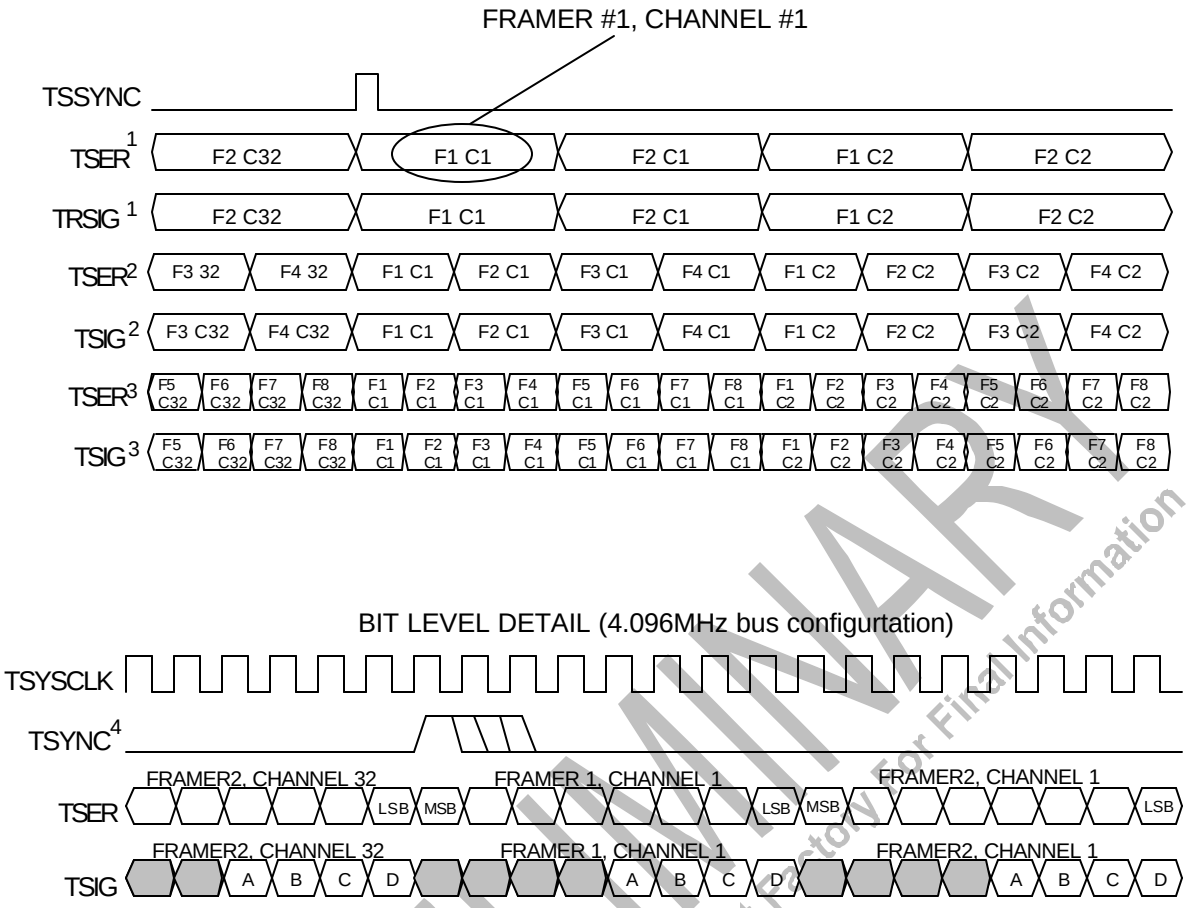
TRANSMIT SIDE BOUNDARY TIMING, TSYSCLK = 2.048MHz (With Elastic Store Enabled) Figure 35-21



NOTE:

1) TCHBLK is programmed to block channel 31.

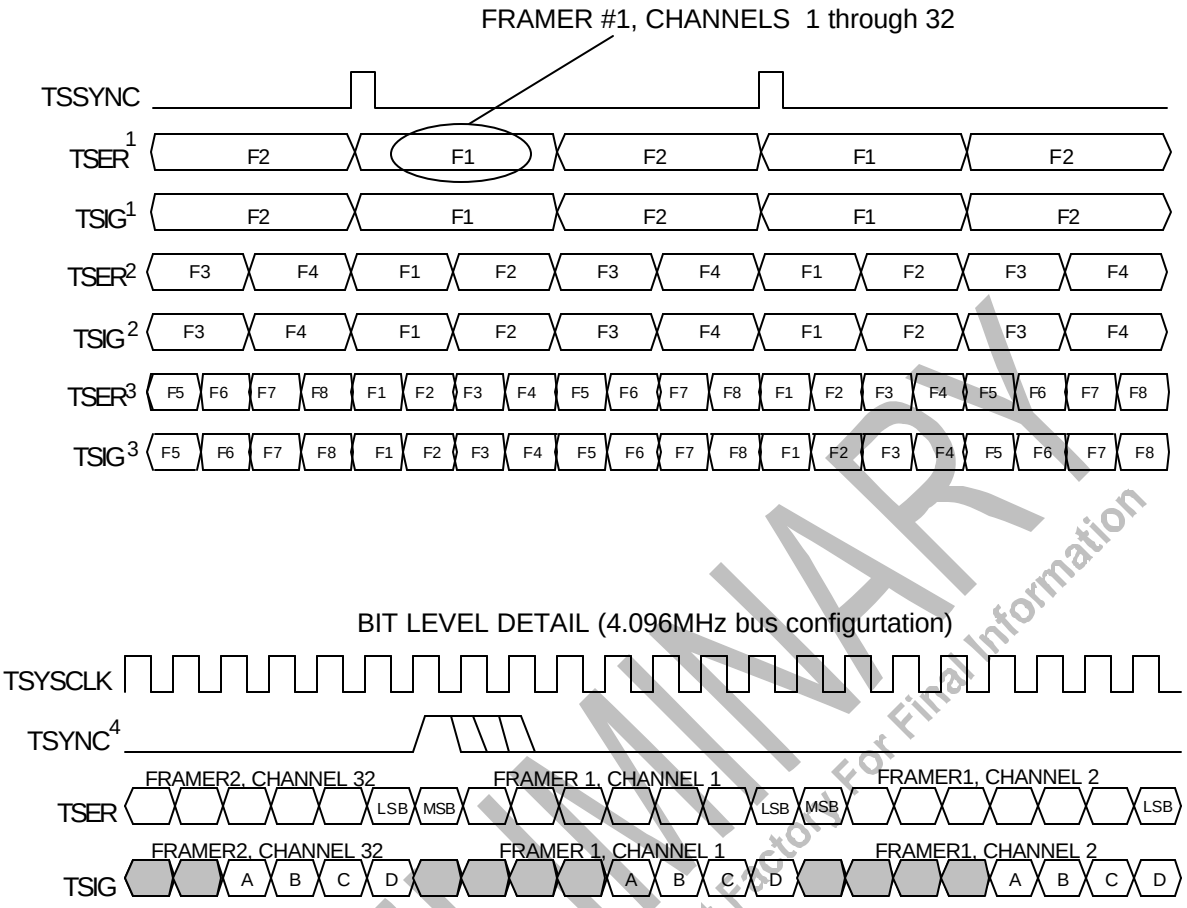
TRANSMIT IBO CHANNEL INTERLEAVE MODE TIMING Figure 35-22



NOTES:

1) 4.096MHz bus configuration.
2) 8.192MHz bus configuration.
3) 16.384MHz bus configuration
4) TSYNC is in input mode

TRANSMIT IBO FRAME INTERLEAVE MODE TIMING Figure 35-23



NOTES:

1) 4.096MHz bus configuration.
2) 8.192MHz bus configuration.
3) 16.384MHz bus configuration
4) TSYNC is in input mode

33. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature Range for DS21Q55	0°C to +70°C
Operating Temperature Range for DS21Q55N	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-20A

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

THERMAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	NOTES
Ambient Temperature	-40°C	-	+85°C	1
Junction Temperature	-	-	+125°C	
Theta-JA (θ_{JA}) in Still Air for 100-pin LQFP	-		-	2
Theta-JA (θ_{JA}) in Still Air for 10mm CSBGA pin LQFP	-		-	2

NOTES:

1) The package is mounted on a four-layer JEDEC standard test board.
2) Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board.

THETA-JA (q_{JA}) vs AIRFLOW

FORCED AIR (meters per second)	THETA-JA (q_{JA}) 100-PIN LQFP	THETA-JA (q_{JA}) 10mm CSBGA
0		
1		
2.5		

RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C for DS21Q55; -40°C to +85°C for DS21Q55N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	3.135	3.3	3.465	V	1

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to +70°C; V_{DD} = 3.3V ± 5% for DS21Q55;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21Q55N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		380		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1) Applies to RV_{DD}, TV_{DD}, and DV_{DD}.
2) TCLK = TCLKI = RCLKI = TSYSCLK = RSYSCLK = MCLK1 = MCLK2 = 1.544MHz; outputs open circuited.
3) $0.0V < V_{IN} < V_{DD}$.
4) Applied to INT* when 3-stated.

34. AC TIMING PARAMETERS AND DIAGRAMS

Capacitive test loads are 40pF for bus signals, 20pF for all others.

34.1 Multipexed Bus AC Characteristics

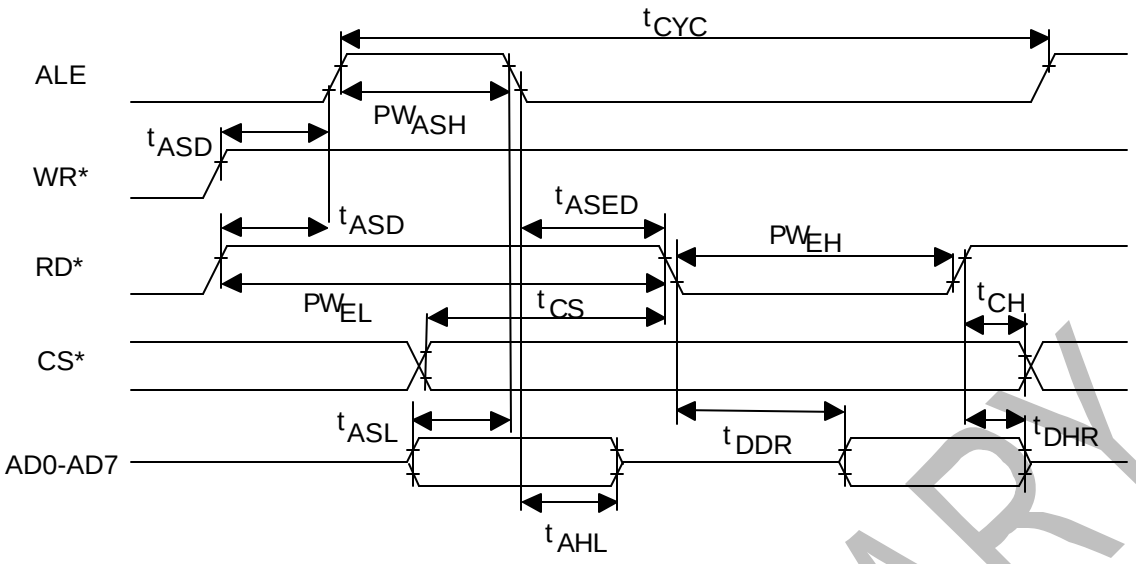
AC CHARACTERISTICS–MULTIPLEXED PARALLEL PORT (MUX = 1)

(0°C to +70°C; V_{DD} = 3.3V ± 5% for DS21Q55;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21Q55N)

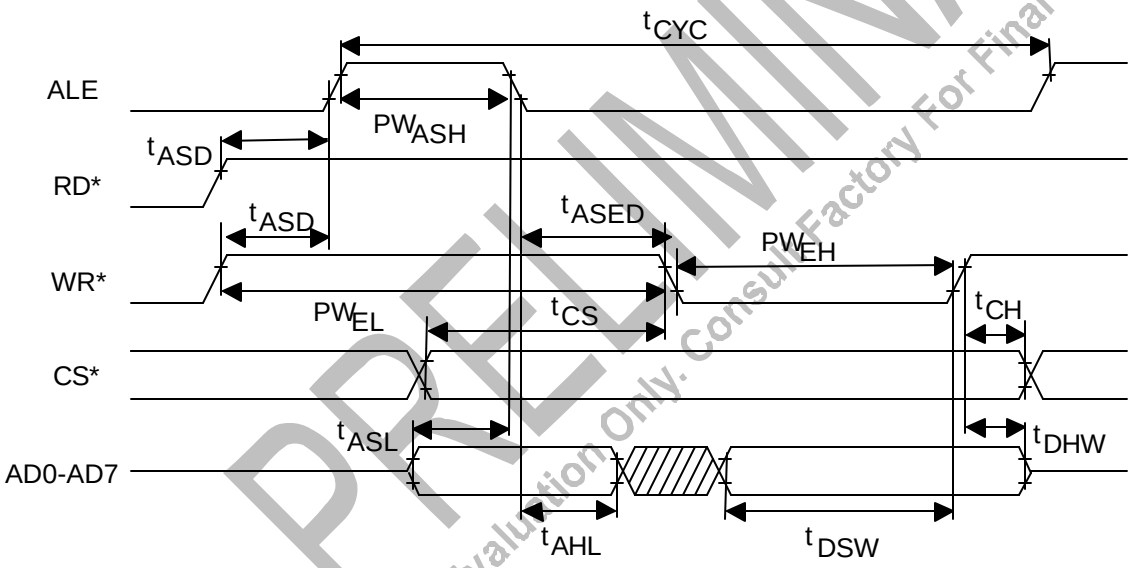
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	T_{CYC}	200			ns	
Pulse Width, DS Low or RD* High	PW_{EL}	100			ns	
Pulse Width, DS High or RD* Low	PW_{EH}	100			ns	
Input Rise/Fall Times	T_R, t_F			20	ns	
R/W* Hold Time	T_{RWH}	10			ns	
R/W* Setup Time Before DS High	T_{RWS}	50			ns	
CS* Setup Time Before DS, WR* or RD* Active	t_{CS}	20			ns	
CS* Hold Time	t_{CH}	0			ns	
Read Data Hold Time	T_{DHR}	10		50	ns	
Write Data Hold Time	T_{DHW}	5			ns	
Muxed Address Valid to AS or ALE Fall	T_{ASL}	15			ns	
Muxed Address Hold Time	T_{AHL}	10			ns	
Delay Time DS, WR*, or RD* to AS or ALE Rise	T_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, WR* or RD*	T_{ASED}	10			ns	
Output Data Delay Time from DS or RD*	T_{DDR}			80	ns	
Data Setup Time	T_{DSW}	50			ns	

See Figures 37-1 to 37-3

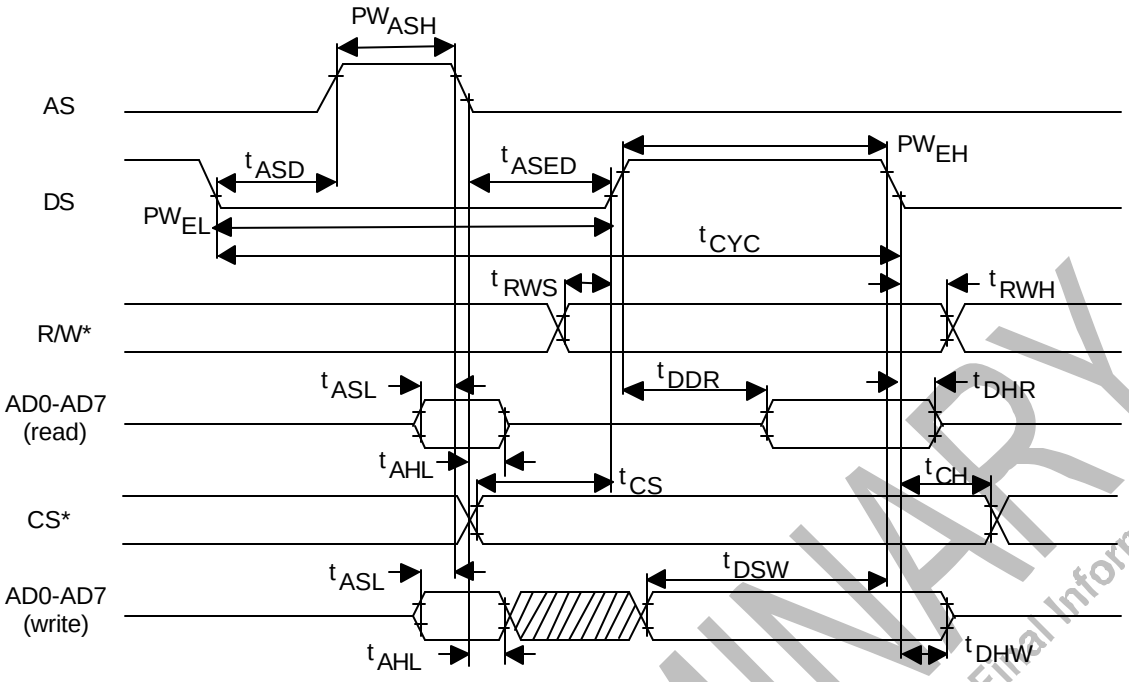
INTEL BUS READ TIMING (BTS = 0 / MUX = 1) Figure 37-1



INTEL BUS WRITE TIMING (BTS = 0 / MUX = 1) Figure 37-2



MOTOROLA BUS TIMING (BTS = 1 / MUX = 1) Figure 37-3



34.2 Nonmultiplexed Bus AC Characteristics

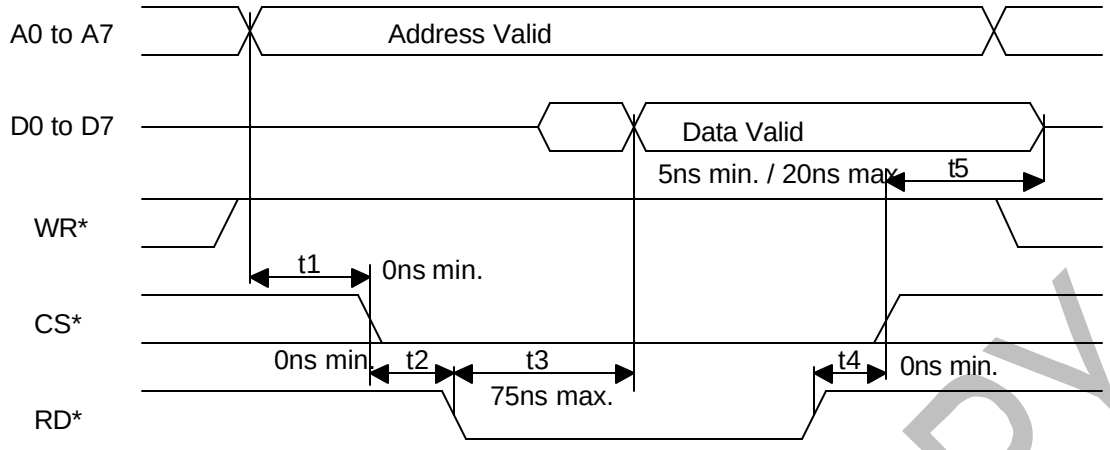
AC CHARACTERISTICS–NONMULTIPLEXED PARALLEL PORT (MUX = 0)

(0°C to +70°C; V_{DD} = 3.3V ± 5% for DS21Q55;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21Q55N)

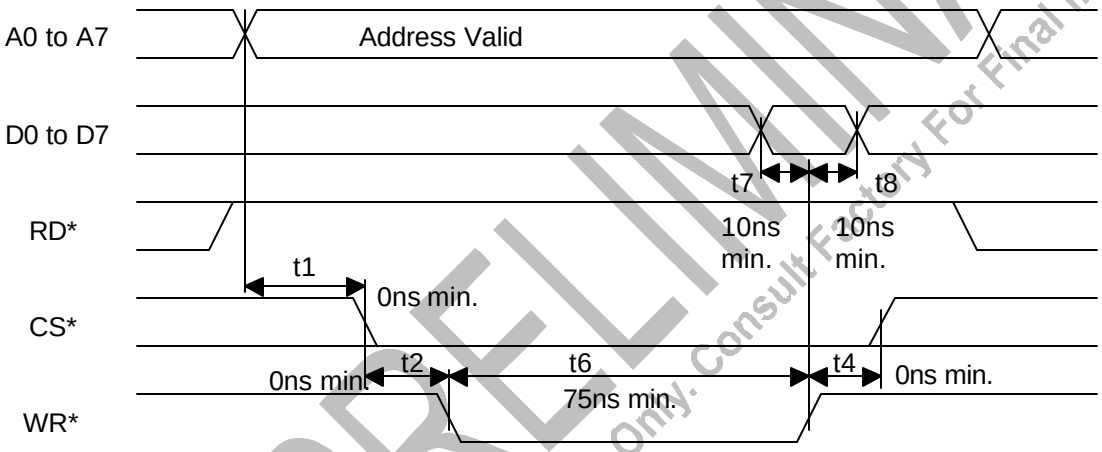
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Setup Time for A0 to A7, Valid to CS* Active	t1	0			ns	
Setup Time for CS* Active to Either RD*, WR*, or DS* Active	t2	0			ns	
Delay Time From Either RD* or DS* Active to Data Valid	t3			75	ns	
Hold Time From Either RD*, WR*, or DS* Inactive to CS* Inactive	t4	0			ns	
Hold Time From CS* Inactive to Data Bus 3-state	t5	5		20	ns	
Wait Time from Either WR* or DS* Activate to Latch Data	t6	75			ns	
Data Setup Time to Either WR* or DS* Inactive	t7	10			ns	
Data Hold Time from Either WR* or DS* Inactive	t8	10			ns	
Address Hold from Either WR* or DS* Inactive	t9	10			ns	

See Figures 37-4 to 37-7

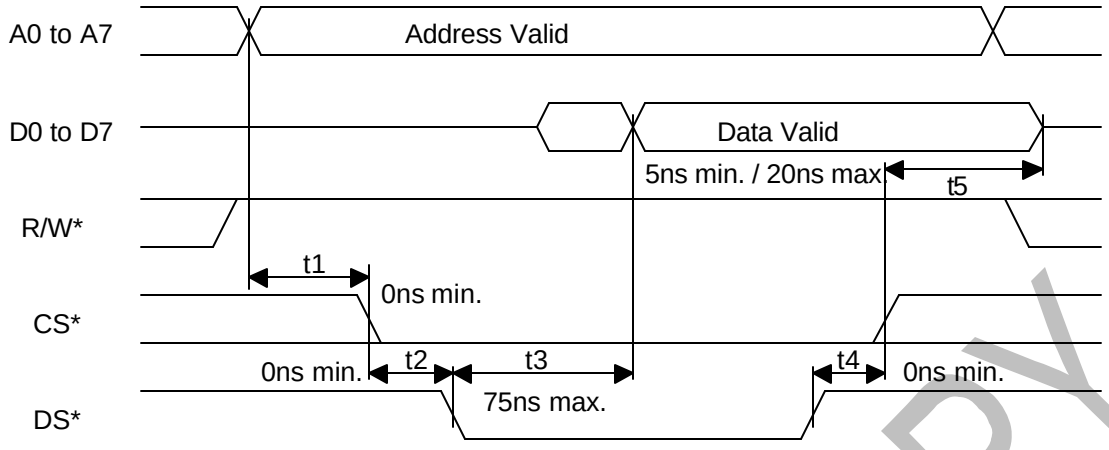
INTEL BUS READ TIMING (BTS = 0 / MUX = 0) Figure 37-4



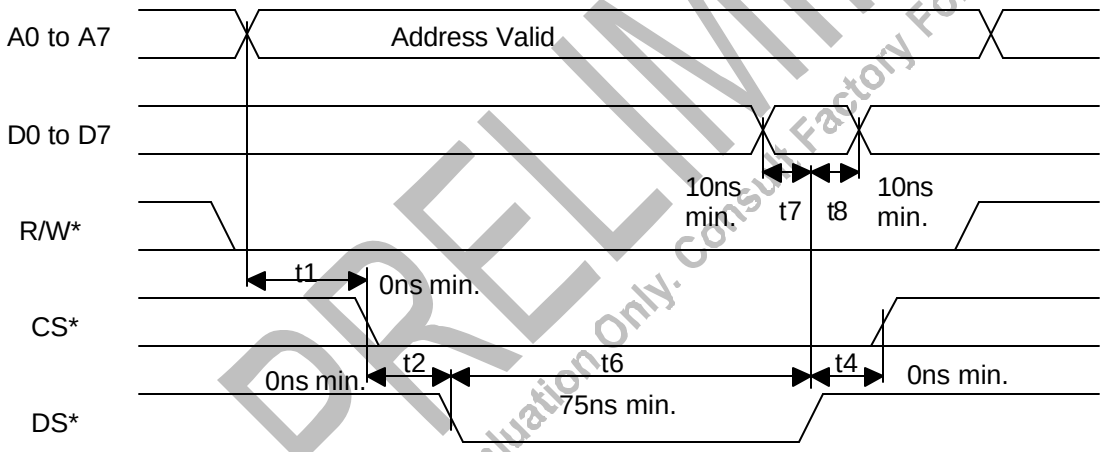
INTEL BUS WRITE TIMING (BTS = 0 / MUX = 0) Figure 37-5



MOTOROLA BUS READ TIMING (BTS = 1 / MUX = 0) Figure 37-6



MOTOROLA BUS WRITE TIMING (BTS = 1 / MUX = 0) Figure 37-7



34.3 Receive Side AC Characteristics

AC CHARACTERISTICS–RECEIVE SIDE

(0°C to +70°C; V_{DD} = 3.3V ± 5% for DS21Q55;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21Q55N)

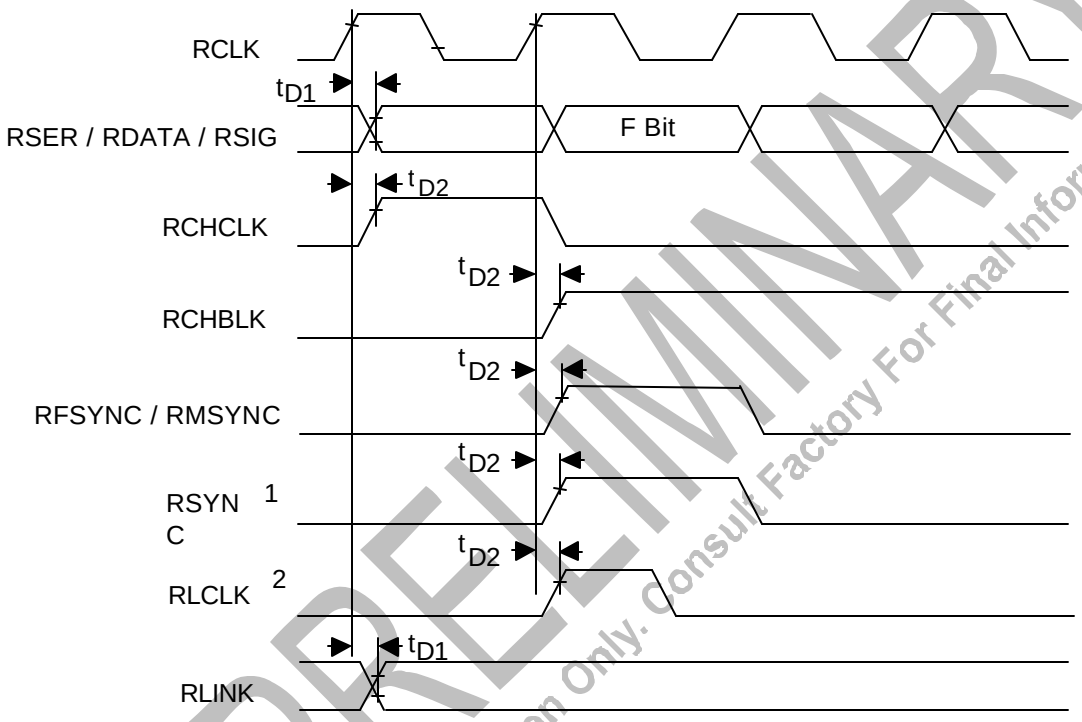
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLKO Period	t_{LP}		488 (E1) 648 (T1)		ns ns	
RCLKO Pulse Width	t_{LH} t_{LL}	200 200	.5 t_{LP} .5 t_{LP}		ns ns	1 1
RCLKO Pulse Width	t_{LH} t_{LL}	150 150	.5 t_{LP} .5 t_{LP}		ns ns	2 2
RCLKI Period	t_{CP}		488 (E1) 648 (T1)		ns	
RCLKI Pulse Width	t_{CH} t_{CL}	20 20	.5 t_{CP} .5 t_{CP}		ns ns	
RSYSCLK Period	t_{SP} t_{SP} t_{SP} t_{SP} t_{SP}		648 488 244 122 61		ns ns	3 4 5 6 7
RSYSCLK Pulse Width	t_{SH} t_{SL}	20 20	.5 t_{SP} .5 t_{SP}		ns ns	
RSYNC Setup to RSYSCLK Falling	t_{SU}	20			ns	
RSYNC Pulse Width	t_{PW}	50			ns	
RPOSI/RNEGI Setup to RCLKI Falling	t_{SU}	20			ns	
RPOSI/RNEGI Hold From RCLKI Falling	t_{HD}	20			ns	
RSYSCLK, RCLKI Rise and Fall Times	t_R, t_F			22	ns	
Delay RCLKO to RPOSO, RNEGO Valid	t_{DD}			50	ns	
Delay RCLK to RSER, RDATA, RSIG, RLINK Valid	t_{D1}			50	ns	
Delay RCLK to RCHCLK, RSYNC, RCHBLK, RFSYNC, RLCLK	t_{D2}			50	ns	
Delay RSYSCLK to RSER, RSIG Valid	t_{D3}			22	ns	
Delay RSYSCLK to RCHCLK, RCHBLK, RMSYNC, RSYNC	t_{D4}			22	ns	

See Figures 37-8 to 37-10

NOTES:

1) Jitter attenuator enabled in the receive path.
2) Jitter attenuator disabled or enabled in the transmit path.
3) RSYSCLK = 1.544MHz.
4) RSYSCLK = 2.048MHz.
5) RSYSCLK = 4.096MHz.
6) RSYSCLK = 8.192MHz.
7) RSYSCLK = 16.384MHz.

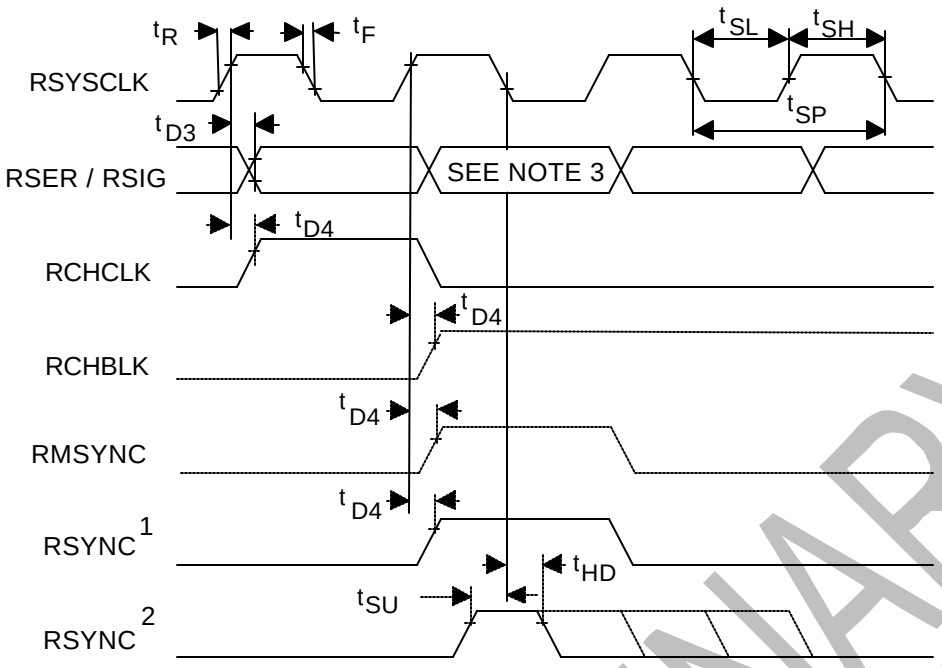
RECEIVE SIDE TIMING (T1 MODE) Figure 37-8



NOTES:

1) RSYNC is in the output mode.
2) Shown is RLINK/RLCLK in the ESF framing mode.
3) No relationship between RCHCLK and RCHBLK and other signals is implied.

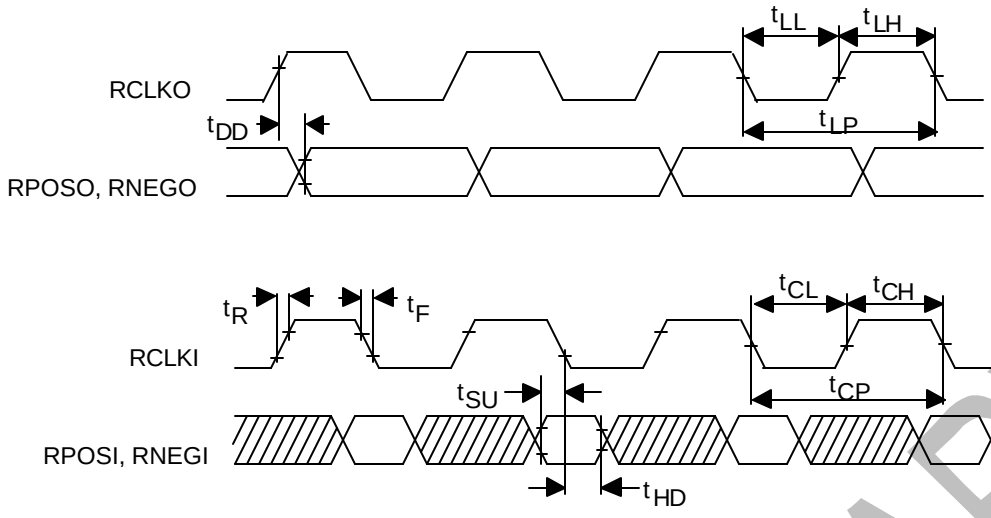
RECEIVE SIDE TIMING, ELASTIC STORE ENABLED (T1 MODE) Figure 37-9



NOTES:

1) RSYNC is in the output mode.
2) RSYNC is in the input mode.
3) F-bit when CCR1.3 = 0, MSB of TS0 when CCR1.3 = 1.

RECEIVE LINE INTERFACE TIMING Figure 37-10



34.4 Transmit AC Characteristics

AC CHARACTERISTICS–TRANSMIT SIDE

(0°C to +70°C; V_{DD} = 3.3V ± 5% for DS21Q55;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21Q55N)

PARAMETER	SYMBOL	MIN	TYP (E1)	MAX	UNITS	NOTES
TCLK Period	t_{CP}		488 (E1) 648 (T1)		ns	
TCLK Pulse Width	t_{CH} t_{CL}	20 20	.5 t_{CP} .5 t_{CP}		ns ns	
TCLKI Period	t_{LP}		488 (E1) 648 (T1)		ns	
TCLKI Pulse Width	t_{LH} t_{LL}	20 20	.5 t_{LP} .5 t_{LP}		ns ns	
TSYSCLK Period	t_{SP} t_{SP} t_{SP} t_{SP} t_{SP}		648 448 244 122 61		ns ns ns ns ns	1 2 3 4 5
TSYSCLK Pulse Width	t_{SP} t_{SP}	20 20	.5 t_{SP} .5 t_{SP}		ns ns	
TSYNC or TSSYNC Setup to TCLK or TSYSCLK Falling	t_{SU}	20			ns	
TSYNC or TSSYNC Pulse Width	t_{PW}	50			ns	
TSER, TSIG, TLINK, TPOSI, TNEGI Set Up to TCLK, TSYSCLK, TCLKI Falling	t_{SU}	20			ns	
TSER, TSIG, TLINK Hold From TCLK or TSYSCLK, Falling	t_{HD}	20			ns	
TPOSI, TNEGI Hold From TCLKI Falling	t_{HD}	20			ns	
TCLK, TCLKI or TSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay TCLKO to TPOSO, TNEGO Valid	t_{DD}			50	ns	
Delay TCLK to TCHBLK, TCHCLK, TSYNC, TLCLK	t_{D2}			50	ns	
Delay TSYSCLK to TCHCLK, TCHBLK	t_{D3}			22	ns	

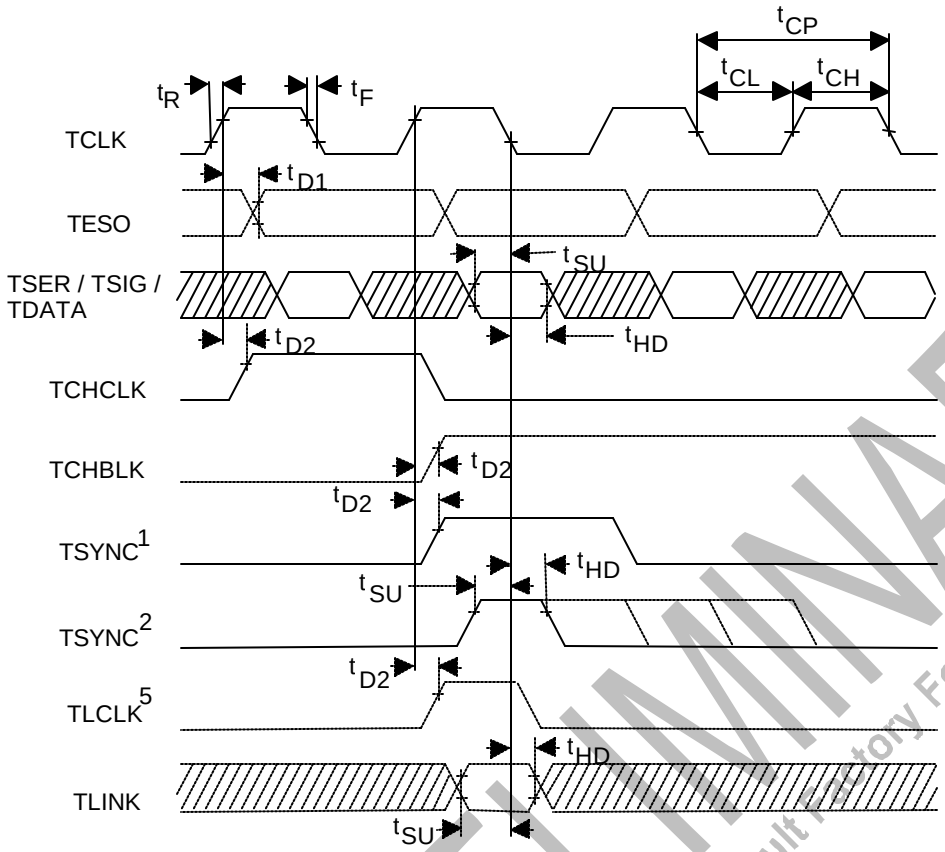
See Figures 37-11 to 37-13

NOTES:

1) TSYSCLK = 1.544MHz.
2) TSYSCLK = 2.048MHz.
3) TSYSCLK = 4.096MHz.

4) TSYSCLK = 8.192MHz.
5) TSYSCLK = 16.384MHz

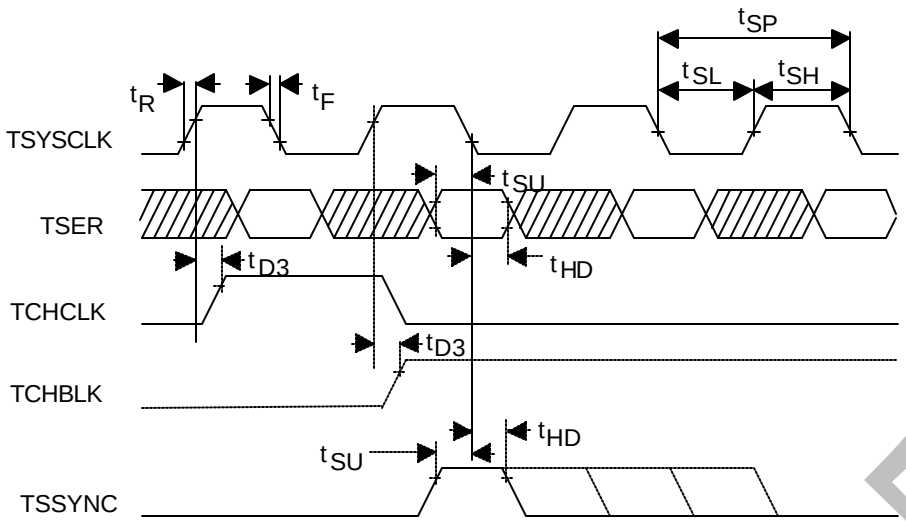
TRANSMIT SIDE TIMING Figure 37-11



NOTES:

1) TSYNC is in the output mode (TCR2.2 = 1).
2) TSYNC is in the input mode (TCR2.2 = 0).
3) TSER is sampled on the falling edge of TCLK when the transmit-side elastic store is disabled.
4) TCHCLK and TCHBLK are synchronous with TCLK when the transmit-side elastic store is disabled.
5) TLINK is only sampled during F-bit locations.
6) No relationship between TCHCLK and TCHBLK and the other signals is implied.

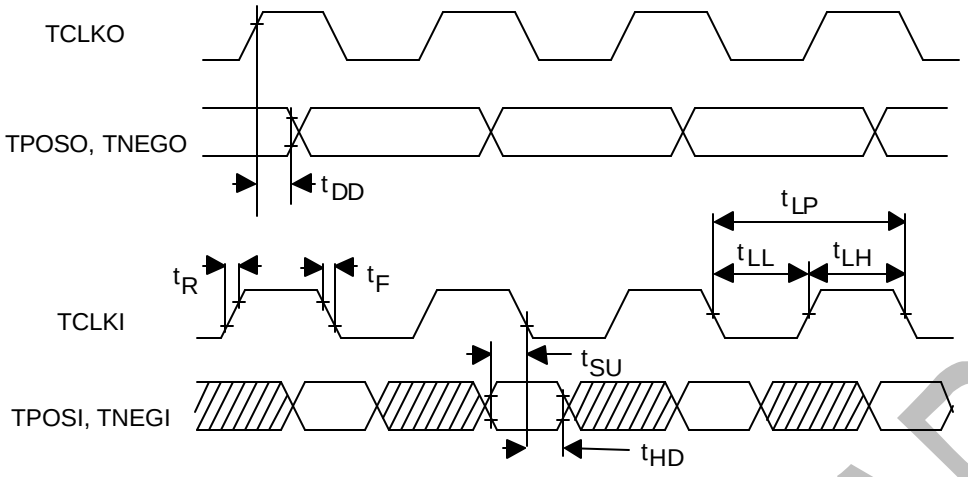
TRANSMIT SIDE TIMING, ELASTIC STORE ENABLED Figure 37-12



NOTES:

1) TSER is only sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.
2) TCHCLK and TCHBLK are synchronous with TSYSCLK when the transmit-side elastic store is enabled.

TRANSMIT LINE INTERFACE TIMING Figure 37-13



35. MECHANICAL DESCRIPTIONS